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Service Manual
$SaO_2/ETCO_2$ Monitor
Model 7000

July 20, 1989

Part Number 5007-90-P3

This manual based on Version 5.7 CPU software.

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Preliminary Documentation

SaO2 Fuse - F1 - 125V, 62ma
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$5.09

SaO2 Span Cell - $212.50 exchange
5218-01
List $425

CO2 Transducer - #4981-37
$495.00 - 90 day warranty
$650.00 - 6 month warranty sp6
#50 credit
$750 - 1 year warranty sp12
#50 credit.
$1395.00 List.

SaO2 probe #8776
$255.00 - 6 month warranty
#5 credit
$295 List.

VHS # 9899506

$445.00

CRT & Board - # 570007
$350.00 - new CRT & Board

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1.0 Theory of Operation

1.1 Introduction

The Model 7000 is a non-invasive portable $SaO_2/ETCO_2$ monitor designed to produce reliable continuous measurement, monitoring, and display of oxygen saturation, pulse rate, expired CO_2, and respiratory rate. This is performed by analyzing the changes in infra-red light sources and computing the results to acquire the correct parameter results. A user friendly menu display system assists in programming the unit for individual requirements, once programmed any changes are permanently stored in memory even after the unit is turned off.

There are five "softkeys" which perform different commands depending upon the present status or menu displayed, this eliminates large confusing keypanels and simplifies the monitor's operation. The front panel is a membrane switch overlay which contains the five softkeys, power switch and indicators, the ALERT RESET and AUDIO buttons, along with the Cal Cell used in calibrating the Capnostat™ CO_2 sensor. The two front panel jacks "SaO_2 INPUT" and "CO_2 INPUT" are for the connection of the two sensors used for the system. The jacks are different to avoid connection of the wrong sensor. All connections are run through the system's Motherboard via removable connectors for ease of disassembly.

The unit can operate from any voltage and frequency found in the world by simply changing a programming key found in the power entry module on the rear panel. A battery backup will supply approximately 1 hour of operation with protection circuitry to prevent possible battery damage.

The monitor is controlled by the Motorola MC68000 Microprocessor which is referred to as the "host". Consider the host as the "brains" of the system, it controls all internal functions through communication with each board, runs the system software, and communicates with external equipment through the rear panel connectors. All communication lines are run through the Motherboard where all the individual circuit boards are housed. The CRT displays the waveforms as selected by the user along with the softkey functions. Various displays are available, each is described thoroughly in the Operating Manual.

The different assemblies found in the Model 7000 are listed below:

- 2401 Power Supply Board
- 2402 CPU Memory Board
- 2403 Main CPU Board
- 2404 Video Controller
- 2421 Digital CO_2 Front End Board (previously 2407)
- 2418 Analog CO_2 Front End Board (previously 2409)
- 2267 Digital SaO_2 Front End Board
- 2268 Analog SaO_2 Front End Board
- Motherboard

- CRT Assembly
- Front Panel Membrane Switch Overlay

1.2 Power Supply # 2401

1.2.1 Output voltages

There are four low level DC voltages supplied as outputs from the 1260/7000 power supply. Three of these voltages (+5V, +15V, -15V) need to be closely regulated since they are used to power critical digital and analog components which make up the heart of the monitor. Even small deviations from their nominal values may lead to erroneous data or even device failure. The fourth voltage (V BAT) need not be as tightly regulated since it is used to power the CRT picture tube and the fan, and under AC operation mode is used to charge the battery. While this voltage may be less regulated it must still be kept within acceptable limits so that the components operate properly.

1.2.2 AC / DC operation

The 1260/7000 monitor can operate either in AC mode by an external connection to an AC power line or in DC mode with its internal battery.

AC operation mode occurs when the monitor is:

- Plugged into a properly wired AC line with an acceptable operating voltage level.
- Both the line cord and fuses are in good condition, and
- the rear panel power entry switch is set ON (|).

DC operating mode occurs when either:

- unit is unplugged from the AC line or the AC voltage is below an acceptable operating level.
- Power cord and/or fuse are bad.
- AC line power is lost, or
- the rear panel power entry switch is set to OFF (O).

While the monitor is connected to an acceptable AC source and the conditions for AC operating mode are met, the monitor operates in AC mode and the internal battery is charged. As soon as the AC line voltage into the monitor falls below the acceptable operating level, or the unit is turned on while not connected to an AC line source, DC operating mode is automatically initiated. When an acceptable AC line is once again introduced into the monitor, AC operating mode is restored. No loss of monitor function or information occurs when switching between AC and DC modes. The AC LED on the front panel indicates that AC power is present.

1.2.3 DC power source

The power source for the DC mode is the internal lead acid battery. To prevent the battery from being ruined by a deep discharge under DC operation, the power supply

turns the monitor of when battery voltage falls to a preset threshold. A "Low Battery" warning is provided to alert the user before the turn off threshold is actually reached. To provide the battery with a quick charge while maintaining stand-by float current for back-up power, a constant voltage charging method is used. The battery delivers between 13.8 volts when it is fully charged down to the turn off threshold of 10.5 VDC.

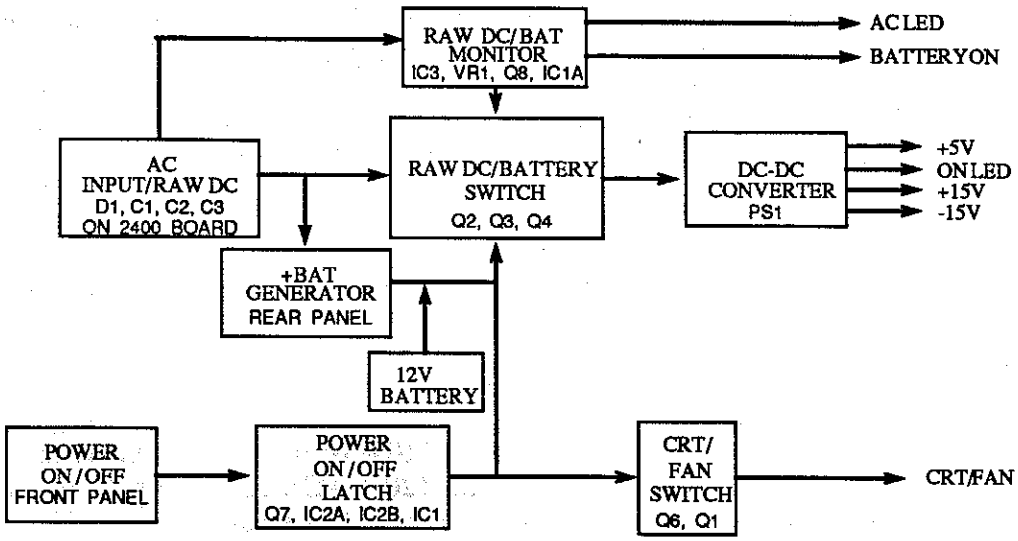
1.2.4 AC power source

AC power input depends on not only the country in which the monitor is used but also how well the power company can regulate their power given the varying demands of their users. The 1260/7000 can switch its primary input between 100, 120, 200, 240 VAC by changing the voltage selector on the rear panel power entry module. A fuse change is also required when going from 100/120 VAC to 200/240 VAC. Voltage fluctuations due to normal power line conditions in excess of 10% of the nominal value are expected and tolerated by the system. For example, with 120 VAC nominal input, the low line voltage is 120 - 10% = 108 VAC and the high-line value is 120 + 10% = 132 VAC.

1.2.5 Block diagram operation

The AC INPUT/RAW DC block converts AC line input into an unregulated DC voltage. RAW DC is fed into the +BAT GENERATOR and the RAW DC/BATTERY SWITCH. The output from the +BAT GENERATOR is used to charge the battery, and is also sent to the RAW DC/BATTERY SWITCH and the CRT/FAN SWITCH. The output of the RAW DC/BATTERY SWITCH is sent into the input of the DC-DC CONVERTER. The RAW DC/BATTERY LINE MONITOR senses the voltage level on both the RAW DC and BATTERY lines and decides whether the RAW DC/BATTERY SWITCH should send RAW DC or BATTERY to the DC-DC CONVERTER. The RAW DC/BATTERY MONITOR also sends a BATTERY ON/OFF signal to the processor as well as controls the AC ON LED on the front membrane keypanel.

The POWER ON/OFF LATCH is activated by the POWER ON/OFF SWITCH located on the front membrane keypanel and generates a POWER ON/OFF SIGNAL. The POWER ON/OFF SIGNAL is used to control the outputs of the CRT/FAN SWITCH and the DC-DC CONVERTER, turning the monitor on and off. The CRT/FAN SWITCH provides power to the CRT tube and to the fan, while the DC-DC CONVERTER provides power for the +5V and the ±15V DC supplies. The +5V output from the DC-DC CONVERTER is also used to generate the POWER ON/OFF SIGNAL for the POWER ON LED on the front membrane keypanel.



1.2.6 AC INPUT/RAW DC block

The AC INPUT/RAW DC block consists of a power entry module, a power transformer, a bridge rectifier, and several capacitors. The power entry module incorporates an integral power switch, voltage selector switch, fuse holder and RFI/ EMI filter, as well as provides a receptacle for the line cord. The dual primary transformer, T1, is wound so that the desired voltage selected into the primary induces at least 15 VAC across the secondary during low-line input conditions. The secondary AC voltage is rectified by bridge D1 to produce a full wave rectified output, which is filtered and smoothed out by capacitors C1, C2, and C3 on the Motherboard to make UNREGULATED RAW DC. For all the following equations, an AC line input voltage of 120 VAC is assumed. The value of RAW DC varies according to the AC line input and the monitor power requirements:

RAW DC (VDC) = Secondary AC voltage (Vrms) / .707
= 15 VAC (min) / .707
= 21 VDC

The maximum magnitude of ripple (AC fluctuation) on RAW DC is related to the maximum DC current draw of the system, the frequency of the ripple (120 Hz for a bridge rectifier) and the value of the filter capacitors:

Vripple (VAC) = Current / (Capacitance * Frequency)
= 4 A / (0.03 F * 120 Hz)
= 1.11 VAC

1.2.7 THE +BAT GENERATOR

To generate the voltage required to charge the battery during AC operation and power the CRT and the fan, an adjustable linear voltage regulator integrated circuit is used. This device is located on the back panel of the monitor which it uses as a heatsink. It takes as its input the UNREGULATED RAW DC and produces a regulated 14.5 VDC at its output. A power diode, D2, protects the IC during battery operation, and allowing for a 0.7 V drop in voltage across the diode, a constant voltage charge of 13.8 VDC (2.3 volts per

battery cell) is present under AC operation. Ultimately, this is voltage dependent upon the condition of the battery and will fluctuate according to the charge of the battery.

1.2.8 AC/BATTERY MONITOR

A dual under/over voltage comparator IC3 (ICL7665), continually monitors the condition of both RAW DC and the BATTERY lines and compares them with an internal 1.3 volt reference. When adequate AC power is present, the RAW DC line (as scaled by the voltage divider consisting of R5 and R6), is above the trip voltage and is used as the primary power source for the monitor. The scaling equation for the RAW DC line is:

RAW DC Trip = ((R5+R6) / R6) * 1.3 V
= ((27.5 + 301) / 27.5) * 1.3 V
= 15.5 VDC

If AC power declines and falls below the trip voltage, the AC/BATTERY MONITOR switches over to DC operation mode. The battery becomes the primary power source, provided it has an adequate charge. As with the RAW DC, the condition of the battery is also sensed through scaling resistors but because it is desired to prevent the battery from becoming deeply discharged, both lower and upper battery trip points are set. The lower trip point sets the voltage at which a low battery condition is detected and the monitor is automatically shut off, while the upper trip point represents the minimum voltage that must be present across the battery terminals before the monitor can be turned on. Taking the diode drop across D1 into consideration, for a nominal lower and upper trip points of 10.5 and 12.0 volts are set by:

Lower Trip = ((R19 + R8 + (1/2 VR1)) / R19) * 1.3 V
= ((200 + 1100 + (1/2) (500)) / 200) * 1.3 V
= 10.075 V

Low Battery = 10.075 + 0.7
= 10.775 V

Upper Trip = ((R19 + R8 + R7 + (1/2 VR1)) / R19)) * 1.3V
= ((200 + 1100 + 200 + (1/2)(500)) / 200) *1.3V
= 11.375 V

Battery On = 11.375 + 0.7
= 12.075 V

Potentiometer VR1 is used to compensate for component tolerances when setting the upper and lower trip voltages. The output state of the dual comparator is also used to provide the logic for turning on the AC LED on the front panel via Q8, and a BATTERY ON signal to the Microprocessor.

1.2.9 RAW DC/BATTERY SWITCH and DC-DC CONVERTER

Under DC operation, the battery is gated to the input of the DC-DC CONVERTER and the monitor is run completely off the internal battery. A logic high at the output of IC1D turns transistor Q4 on, bringing the base of transistor Q3 low and turning it on.

Transistor Q3 then turns power transistor Q2 fully on, and it acts as a low impedance switch for the battery into the CONVERTER. Back biased diode D3 prevents battery power from leaking back into the RAW DC line. When adequate RAW DC is present, transistor switch Q2 is off and D3 is forward-biased, sending RAW DC onto the CONVERTER. The DC-DC CONVERTER is a 50 Watt switching power supply which can convert a 9 to 24 volt input into tightly regulated +5, +15, and -15 VDC outputs with an efficiency of about 75%. The outputs of the converter are enabled directly by an ON signal from IC1C, the POWER ON / OFF LATCH. The +5v supply line with R25 is used to signal the monitor is on via the ON LED located on the front panel.

1.2.10 CRT/FAN SWITCH

To avoid the loss of efficiency when going through the DC-DC Converter and since the CRT and the fan require only loosely regulated input power, FET switch Q1 and its associated circuitry is used to supply the CRT display and the fan directly from the +BAT line. Because the FET has very low resistance when turned on, very little power is lost in the switch and wasted when the CRT tube and fan are on, which is an important consideration given the high power requirements of the CRT. The switch is controlled directly off of IC1B of the POWER ON/OFF LATCH.

1.2.11 POWER ON/OFF LATCH

The POWER ON/OFF LATCH receives its control from a pulse generated during the closure of the front panel POWER key, which appears at the collector of Q7. This pulse, whose width is controlled by capacitor C1 and resistor R3, is debounced by the first D flip-flop (IC2A), and a short pulse is generated at the Q not output. The positive edge of this pulse causes the output of the second D flip-flop (IC2B) to toggle and to latch onto the present state until the next positive clock edge. In the event that a low battery condition is detected by the RAW DC/BATTERY MONITOR, the output of the POWER ON/OFF LATCH will be forced to the OFF state by transistor Q5 and resistor R13. Capacitor C2 and resistor R17 cause the LATCH to be reset in the OFF state during power-up.

1.3 CPU Memory # 2402

1.3.1 Memory

Two types of memory devices are used, EPROM (IC2, 3, 4, and 5) for program storage, and SRAM (SIMM boards) for temporary storage of variables and trending information. The SRAM is contained on two 2405-01 SIMM boards, one handles the upper byte (128K X 8) and is enabled by the UBRE line, the other handles the lower byte (128K X 8) and is enabled by the LBRE line. The EPROM devices IC2-IC5 are broken up in a similar manner. U2 which consists of two chips (low and high), and U3 (two chips, low and high).

1.3.2 Analog to Digital Converter

The analog to digital converter IC35 has a multiplexed input which reads one of four inputs at a time. When the CS11 line is low IC49 will be enabled on the positive going transition of the LBWE line. Data lines DØ-D3 feed IC49 which transfers the data to the

multiplexor IC34 (which selects one of four analog inputs). The two analog inputs are amplified by IC28A pin 1 and IC28B pin 7, IC28D pin 14 is a spare input. Battery voltage monitoring is handled by IC28C pin 8. IC41 develops a -10 volts VREF for use by IC28 and IC35.

1.4 Main CPU Board # 2403

1.4.1 The Microprocessor

The heart if the system is the Motorola MC68000 MPU which runs at 10 MHz (8 MHz for earlier units). The MC68000 oversees all aspects of the system, from fetching a program instruction and interpreting it to deciding what action to take and informing the peripheral affected by the instruction of its task. The microprocessor communicates with the rest of the system via a 16-bit data bus, which allows information to be transferred in packets that are either one word (the full 16-bits) or one byte (either the high or low 8-bits of the word) in length and a 24-bit address bus that allows the processor to access 16 Mbytes of continuous memory space. The Front End Boards communicate by serial protocol.

The MC68000 has various control lines which provide "handshaking" between the external hardware and the microprocessor to ensure that data transfer and system functions are conducted in a smooth and orderly manner:

R/W (Read/Write) indicates the direction of data transfer. R=Read, data to be sent from the external device to the microprocessor. W=Write, data to be sent from the microprocessor to the external device.

AS (Address Strobe) indicates that a valid address has been placed on the address bus by the microprocessor and signals the start of a data transfer cycle.

UDS, LDS are Upper and Lower Data Strobes, they indicate the length of the packet of data to be transferred. These signals are gated along with R/W by IC31, IC32B, IC30C, and IC36F to develop the LBWE (Lower Byte Write Enable), UBWE

LDS: only the lower byte of the data word contains valid information, the upper 8-bits should be ignored.

UDS: only the upper 8-bits contain valid information, ignore the lower 8-bits.

UDS and LDS together: the full data word contains valid information.

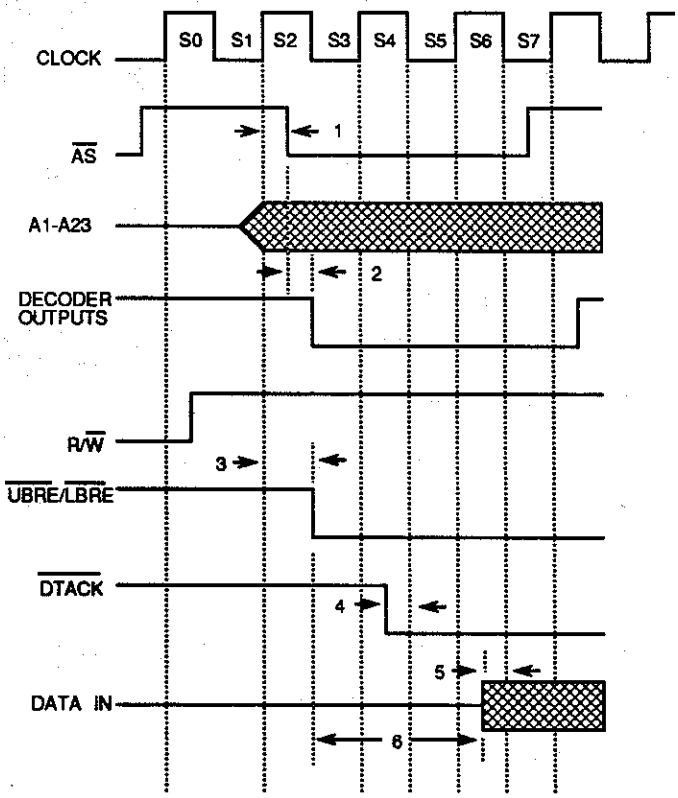
DTACK (Data Transfer ACKnowledge), sent from the external device addressed by the microprocessor to signal that the data sent by the microprocessor has been received by the device.

VPA (Valid Peripheral Address) instructs the processor to obtain an interrupt address from a jump table in ROM, rather than from the address bus.

CLK (system CLocK), governs the basic unit of time for data transfer cycles. This signal is developed from Y1 a 16 MHz oscillator which is divided down by IC37B.

There are three basic types of bus cycles, classified by the direction of data transfer. These are the Read Bus Cycle, where data is transferred from the addressed external device to the microprocessor, the Write Bus Cycle, which transfers data from the microprocessor to the device, and a Read-Modify-Write Bus Cycle where the microprocessor reads data from a device, modifies it according to the program instruction and returns the modified data to the same address.

A Read Bus Cycle occurs either when the microprocessor is ready for the next program step from ROM, needs to retrieve a stored variable in the RAM, or needs to access information from a peripheral. The cycle is started by the microprocessor bringing the Read/Write signal high and letting the device address know the length of the data packet it requires by asserting the appropriate Data Strobe lines. The device responds by placing the data on the data bus and asserting its DTACK line, letting the processor know that the data requested is available. The microprocessor gets the data from the bus, deasserts the handshaking lines, and removes the address from the bus.



S=60 nsec

1-Address Strobe Delay = 60 nsec

2-Decoder Prop Delay = 3 decoder delays = 21 ns

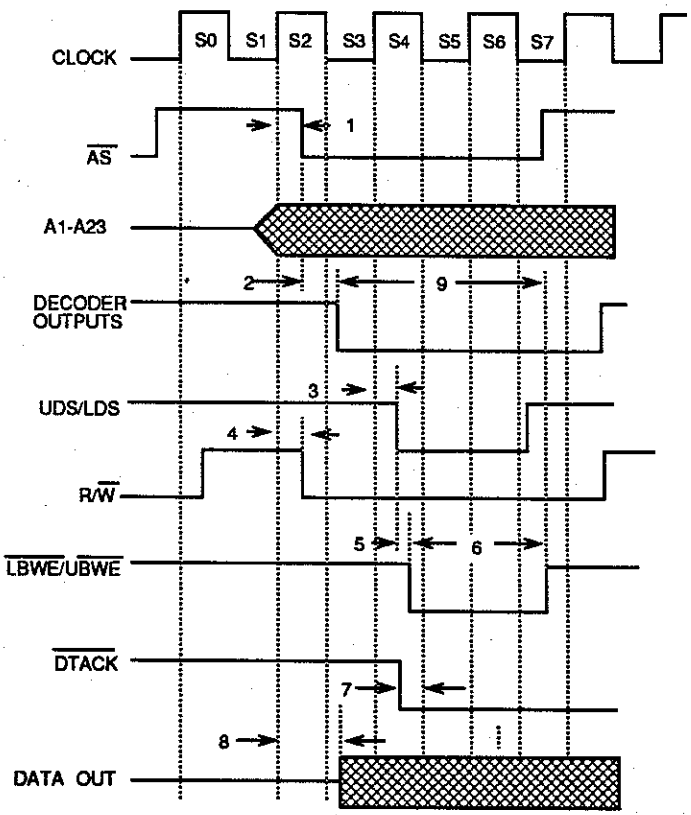
3-UBRE/LBRE Prop Delay = Add Strobe Delay + Dec Prop Delay = 67 ns

4-DTACK Setup = 20 nsec

5-Data Setup Time = 15 nsec

6-Memory Access Time = S2 + S3 + S4 + S5 + S6 - 3 - 5 = 218 nsec

A Write Bus Cycle occurs when the microprocessor needs to store a variable in the RAM or wants to send data to a peripheral. After the address is placed on the bus and Address Strobe is asserted, the Read/Write line is brought low. The data is then placed on the data bus and the appropriate Data Strobes are asserted, writing the information into the addressed device. After successfully receiving the data, the device responds by asserting DTACK and the processor clears the control signals, finally removing the address and data from their busses.



S=60 nsec

1-Address Strobe Delay = 60 nsec

2-Decoder Prop Delay = 21 ns

3-UDS/LDS from S4 = 60 ns

4-R/W from S2 = 70 ns

5-LBRE/UBRE prop delay = 7 ns

6-LBRE/UBRE pulse width = 115 ns

7-DTACK setup = 130 ns

8-Data Setup = 130 ns

9-CE pulse width = (S2 + S3 + 3 + 5 + 6) - (1 + 2) = 221 ns

A Read-Modify-Write Bus Cycle combines the separate Read and Write Cycles into a single coordinated cycle. In the first part of the cycle, data is read from the device in a manner similar to a Read Cycle, except Address Strobe is not de-asserted at the end of the read and the original address remains on the bus. The data is modified by the processor's internal registers and logic unit, and the Read/Write line is brought low, initiating the Write Cycle. The modified data is put on the bus and a write operation is performed at the original address with the assertion of the Data Strobe lines. After the device asserts DTACK, the processor removes the address from the bus, releases the control lines, including Address Strobe and removes the modified data.

1.4.2 Reset

RESET (system RESET) causes initialization of the system either by an external device on power up or if something causes the microprocessor to become lost. This is accomplished by IC39A , when power is applied C4 will charge up through R2 bringing pin 2 high, this will cause pin 4 to generate a 100 msec low pulse (time constant of R2 and C4) after the power and system clock have stabilized. Watchdog circuitry that continuously monitors the processor will also reset the system if a bad instruction or a bus fault cause the processor to get lost.

1.4.3 Status Lines

FCO, FC1, FC2 (Function Code output) indicates the internal state of the processor, the Supervisor State (all of the microprocessors resources are available), or the User State (some of the more sensitive aspects of the system are inaccessible and protected). The signals are gated together by IC40B whose output (pin 6) is the INT (INterrpuT decoder) line.

1.4.4 The Interrupt Lines

IPLO, IPL1, IPL2 (Interrupt Priority Level) are initiated by the external device to let the microprocessor know that the device either has information for the MPU or needs assistance from the microprocessor. IC27 receives the interrupt signal from the device and decodes the output to the IPL lines.

When a request for servicing comes in on the interrupt lines the processor finishes the current instruction then saves it's place in the program on the system stack. It then decodes the IPL lines to find which device has requested assistance and gets the address of the interrupt servicing routine for that device from a lookup table. The processor runs the interrupt service routine, performing the task that the interrupting device needed. If another interrupt of higher priority comes in before the processor is done, the current interrupt service routine is halted at the end of the current instruction, the program location and status are placed on the stack, and the new interrupt is serviced. The new service routine is run and unless a higher priority comes in, it is finished. The location and status of the old service's routine is then removed from the stack and completed. Finally, the original program's place and status are returned from the stack and the processor continues running where it left off before servicing the interrupts.

1.4.5 Timekeeper RAM

The Timekeeper RAM IC14 (MK48T02B-15) combines a Real-Time Clock with 2 Kilobytes of low power CMOS static RAM. Inside the device is a crystal for the clock, a long-life lithium battery, and switching circuitry that provides uninterrupted power to keep any information stored safe and intact when the monitor is turned off. In addition to providing time and date stamping of trend and other output data, the battery backed SRAM is also used to remember the system parameters currently in use. Each time the monitor is turned on, the program restores the saved settings and monitor features. In this way, each time the monitor is powered up, the system parameters and features previously set are maintained and need not be reset by the user

1.4.6 Digital to Analog Converter

The D-to-A Converter (DAC) IC15 (AD7226KN) performs the conversion of information from the digital form the processor uses to an analog voltage between 0 and 10 volts. The AD7226KN is an 8-bit quad DAC providing four separate analog output channels from a shared time-multiplexed input data bus. The processor selects the DAC by addressing IC26 which then sends pin 2 low, and LBWE low. This causes IC32C to go low which activates the WR (WRite) line of IC35. Address lines AØ and A1 (pins 17 and 16 respectively) steer the digital input to the appropriate analog output Va, Vb, Vc, or Vd (pins 2, 1, 20, 19 of IC35 respectively).

1.4.7 Dual Asynchronous Communication Interface Adaptors

The Dual Asynchronous Communication Interface Adaptors R68C552J IC16 and IC17 (abbreviated DACIA) interfaces the serial input it receives with the microprocessor's parallel bus. It also provides data transfer in the opposite direction, taking parallel information from the bus and converting it into a serial bit stream. To coordinate the information exchange between the two computer systems, the DACIA handles handshaking signals between it and the other system and uses the interrupt procedure through IC29B and C to inform the processor that the data has arrived.

There are two DACIAs in the system and each has two separate serial channels. One DACIA (IC16), is used to communicate with external serial devices via IC18 and IC19 which are connected to one of two standard 25 pin D-connectors on the rear panel of the monitor. The other DACIA IC17 is used for internal communication and is used to reduce the number of bus lines required to talk with the front end boards. This simplifies the communication interface between the front-end board's microcontroller and the main microprocessor. Its timing is generated by Y2 a 3.6864 MHz crystal.

1.4.8 Parallel Interface / Timer

The Parallel Interface/Timer (MK68230Q-8D) IC21 is used to provide a general interface between the lower 8-bits of the MC68000 data bus and bits and pieces of the external logic and devices. This peripheral is used to clean-up many details of the system which would otherwise require handling by discrete logic and which would need more microprocessor guidance. The device also increases the flexibility of the interface since it is completely programmable and is able to alter its I/O function as the system requires. Through its bidirectional output port lines, such varied functions as the front panel mem-

brane keys, the battery state, and the I/O mux lines are monitored and interrupts are generated if activity is detected on the lines. Also generated is the timer output (TOUT), which the microprocessor uses as a time base for marking the occurrence of certain events that are controlled by software.

1.4.9 Cal switches

The four DIP switches (S1) on the CPU board are used to define and set certain system parameters. These switches allow the processor to recognize different hardware configurations and alter the program if needed so the appropriate actions are taken depending on the system hardware which is present. IC48 is enabled when IC26 pin 6 (CS6) and the LBRE lines are low, this causes IC33D pin 11 to go low. The condition of S1's switches are then present on DØ-D7 to be read by the processor.

1.4.10 Sound Generator

The SN76476N programmable sound generator IC46 gives the system audio capabilities in addition to the video output of the CRT display. When pin 8 of IC26 goes low, and the LBWE line is low, IC46 is enabled and receives input from data lines DØ-D7. IC46 pin 7 drives IC50B pin 5, which in turn drives Q1, if Q1 is enabled the speaker may sound. IC50A prevents audio output until the junction of R49 and C65 charges past the 4.15 volt threshold on pin 3 of IC50A (junction of R51 and R52). When pin 1 of IC50A goes low (after time constant of R49 and C65) Q2 is turned on and audio may pass to the speaker. The READY line of IC46 pin 4 drives IC43D which is gated with the SOUND GEN CS line by IC40C, it is then inverted by IC43A which develops the TONE DTACK line for the processor.

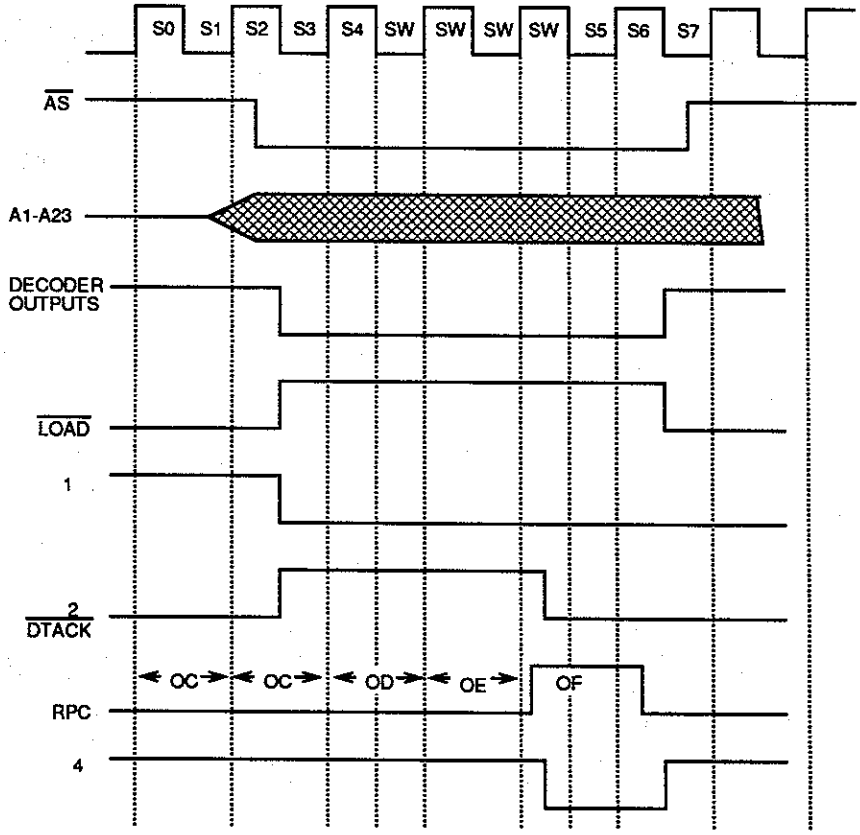
1.4.11 LED latch

The LED latch IC44 lets the microprocessor control the state of the front panel LEDs and then maintains that state without further input from the microprocessor. The current to the LEDs is limited by R32-R41 and switched by 5 transistor array Q3 (CA3046). When the processor addresses IC26 pin 9 (LATCHES) and LBWE go low, IC24C pin 8 goes low which enables IC44. The processor then writes to IC44 on data lines DØ-D7, this data is then latched by IC44 until written to again.

1.4.12 Wait State Generator

Running at 8 MHz, the MC68000 does not allow some of its peripherals enough time in a normal bus cycle to collect, convert and present the requested data. To alleviate this problem, peripherals in the MC68000 family have a DTACK control line to let the processor know when some extra time is required and that it should wait for the device to signal when it is ready for the processor to proceed. This synchronizes data transfer and ensures that only valid information is given to the processor. Not all of the peripherals in this system are of the MC68000 family and do not provide a DTACK signal. To correct this a circuit called a programmable Wait State Generator takes control and can be varied to satisfy the requirements of the individual devices. If a device has its own DTACK line,

then that supersedes the Wait State generated signal so that the processor can process the data as soon as it is available.



1.5 Video Controller # 2404

1.5.1 Introduction

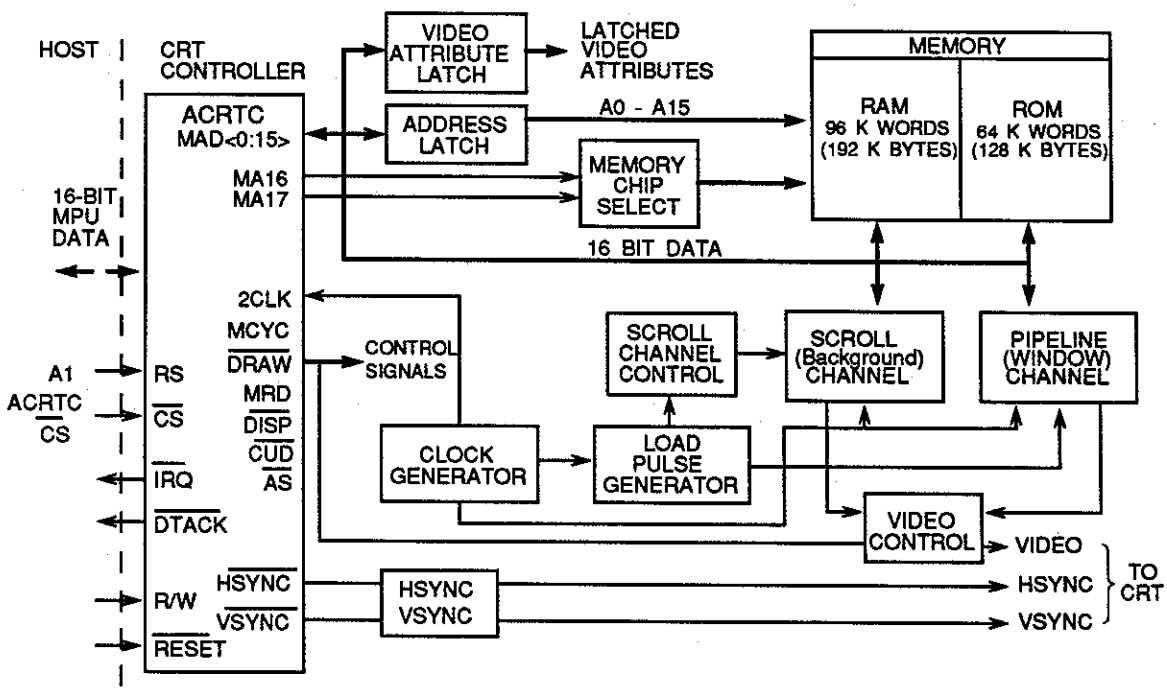
The video display system was designed to provide a high resolution, highly visual display for a medical monitoring device. The heart of the video display system is the Hitachi HD63484 Advanced CRT Controller (ACRTC). Different operating modes allow for long distance viewing of important parameters, detailed views of current physiology, and trend history of stored waveforms. All display modes and user variable settings are menu driven.

1.5.2 Block diagram operation

The ACRTC handles most of the system interface between the microprocessor (Host) and the CRT. The interface between the ACRTC and the CRT (including Video MEMORY) manages the control and timing signals for the CRT and the Video Frame Buffer data. The system timing is generated by CLOCK GENERATOR which produces the 5 MHz 2CLK signal for the ACRTC, LOAD PULSE GENERATOR, SCROLL CHANNEL, and PIPELINE CHANNEL. Both HSYNC and VSYNC, the vertical and horizontal sync pulses, are generated by the ACRTC's Timing Processor and are fed to the CRT.

The MAD lines (0-15) may contain either address, data, or video attribute information depending upon the CONTROL SIGNALS. When address information is present ADDRESS LATCH grabs and holds the data for a read cycle. A similar operation occurs with the VIDEO ATTRIBUTE LATCH when video attribute information is present on the MAD lines. The MEMORY CHIP SELECT enables the appropriate chips when a valid address is on the MAD lines and accessing Frame Buffer MEMORY.

The data flow from MEMORY is determined by the LOAD PULSE GENERATOR which controls the data flow through the SCROLL CHANNEL and PIPELINE CHANNEL which in turn take the parallel MEMORY data off the MAD lines and feed it serially through the VIDEO CONTROL to the CRT.



1.5.3 ACRTC-Host microprocessor system interface

The host to the ACRTC is the Motorola MC68000 16-bit microprocessor which runs at a speed of 8 MHz. The Host communicates with the ACRTC through a 16-bit data bus and a few control signals. The ACRTC appears as a peripheral on the bus occupying 2 address spaces. To access the ACRTC the Host selects the ACRTC base address by the proper decoding of address lines, chooses one of the 2 ACRTC specific addresses and uses the R/W line to signify data direction (either "read" or "write"). The ACRTC responds through DTACK (DaTa ACKnowledge) to signify that it is ready to receive or transmit data. Data is then placed on the bus and this completes either the read or write cycle. The ACRTC register selection is specified by the RS line on the ACRTC which is tied to the low order address line in the 68000.

Instead of waiting for the Host to talk to the ACRTC, the ACRTC can initiate the cycle by sending the 68000 a IRQ which informs the microprocessor that a preprogrammed condition has occurred which needs to be taken care of as soon as possible.

After receiving an IRQ from the ACRTC the Host addresses the ACRTC Status Register to find out the cause of the interrupt.

Also on the microprocessor side of the ACRTC is the reset line control line. When power is first applied, the ACRTC needs to be placed into a known, predefined state so the proper initialization sequence can take place. Pulling the RES line low on power-up, the system gives the ACRTC a hardware reset. When the ACRTC is reset it looks at the DACK (Dma ACKnowledge) line which is tied high to tell the ACRTC that the system has a 16-bit data bus as opposed to 8-bit.

1.5.4 The ACRTC-CRT interface

The CRT interface includes the signals generated by the ACRTC and the hardware used to assist the ACRTC in controlling the CRT. The ACRTC internal processors generate the timing and control signals needed to execute the Host system's commands while the external hardware provides the required logic between the ACRTC and the CRT.

The Video Frame Buffer Memory is managed by the Drawing Processor during drawing cycles. Under its control are the multiplexed address and data lines, the raster address lines, the memory read line and the display drawing line.

> MAD and MA lines provide either Frame Buffer Data, Frame Buffer Address, Raster Address, or Attribute information depending on present state of the ACRTC needed for manipulating the Frame Buffer. Separate latches in the hardware capture the current address and attribute status so they remain valid during the cycle.
>
> MRD (Memory ReaD) line indicates the direction of data flow between the ACRTC and the Frame Buffer during memory drawing cycles and indicates whether the background or window screens are displayed in the superimposed display mode to enable load pulses of the video pipeline shift registers.
>
> DRAW works with MRD to define ACRTC Frame Buffer drawing cycles, and with HSYNC to inhibit load pulse generation in non-display periods.

It is the responsibility of the Display Processor to manage the Frame Buffer during display cycles. In addition to the MAD and MA lines the processor also controls the cursors and character/graphic signal.

> MAD and MA lines during display cycles.
>
> CUD 1 & 2 are the cursor generation signals. The system uses these signals to produce a blinking background area under the window in the superimposed mode.

The generation of the ACRTC timing signals for the CRT depends on the values programmed into the timing control registers and 2CLK.

> 2CLK is the basic ACRTC clock and is derived from the Dot Clock. All timing events can be traced back to this clock source. The Dot

Clock runs at 20 MHz and the 2CLK runs at 5 MHz. It is 2CLK that is used to latch the video attributes, control memory chip selects and enable load pulses.

MCYC is manufactured by the ACRTC at 1/2 2CLK (2.5 MHz), this is used to control memory chip selects and enable load pulses.

AS (Address Strobe) signifies that a valid Frame Buffer address has been placed on the MAD lines. AS is used to latch the Frame Buffer address and provide qualification to chip selects and load pulse generation.

HSYNC is the horizontal sync pulse to indicate the end of a current display line and that horizontal retrace should occur to bring the video beam to the start of the next line. HSYNC is also used with DRAW to inhibit load pulses during non-display periods and with 2CLK to latch the video attributes at the beginning of each new CRT scan line.

VSYNC is the vertical sync pulse. This is set to 57 Hz to present a flicker free display.

DISP 1 & 2 are the active video signals. They are used to blank the video signal during retrace periods.

1.5.5 ADDRESS LATCH

To make efficient use of available IC pins the video attributes, Frame Buffer address, and data share the MAD signal lines and are put on these lines at different times. During a Frame Buffer access, the ACRTC puts out the address for the first half of the cycle and then puts out the data. The address must be held and saved at this point to select the proper memory location for the data transfer. To signify the point in the cycle when the address is valid, the ACRTC provides a signal called the Address Strobe (AS) which is used to control hardware latches IC2 and IC3 to capture and hold the address while data is placed on the lines. Inverter IC24C is used to change the polarity of AS for IC's 2 and 3.

1.5.6 VIDEO ATTRIBUTE LATCH

The Video Attributes are saved in a similar way as explained in section 1.4.5. The MAD lines carry the Attributes during the last 2CLK period of HSYNC and need to be held for the entire raster line. IC11C and IC25D combine HSYNC and 2CLK to produce a pulse for latches IC4 and IC5 which capture the Attributes when they become valid.

1.5.7 MEMORY CHIP SELECT

When a Frame Buffer access is requested, one memory chip pair out of several must be selected (chips are accessed in pairs to provide 16-bits of data for the ACRTC, with one chip supplying the lower 8-bits and the other the upper 8-bits). The decoder IC8A uses higher order address lines to partition the available memory space into RAM and EPROM regions, with each memory chip pair given a unique base starting address. IC11A and IC9B provide a validation signal by gating MCYC, 2CLK, and AS (a chip

select pulse can only be generated if the ACRTC has asserted AS), signifying that a valid address has been placed on the MAD lines. Gates IC24D, E, F; IC13A, B, C; IC14B and IC11D serve to clock validated chip select pulses from the address decoder to the memory at the proper time.

The RAMs need to know if the ACRTC is executing a memory read cycle which transfers data from the memory to the ACRTC, or a memory write cycle which will place new data into the RAM from the Drawing Processor. By combining the MRD and DRAW signals the circuitry creates a data direction signal which is high for memory reads and low for memory writes.

1.5.8 MEMORY

The Frame Buffer contains two types of memory: RAM and EPROM. RAM memory is volatile (it can be read and written to repeatedly but looses its data with power removal). The RAM space is used as video memory to hold dynamic screen displays. The EPROMS are not so volatile. Data placed in them will not be lost unless the chip is intentionally removed from the circuit to be reprogrammed. The EPROMS are used to hold fonts and other static information which needs to be used over and over again. There are 64 K words of RAM and 64 K words of EPROM located in the first half of the 2 Megawords of addressable ACRTC memory.

1.5.9 CLOCK GENERATION

The entire ACRTC circuitry runs synchronously off the 2CLK which is the master timing pulse derived directly from the Dot Clock oscillator. The 20 MHz Dot Clock is divided by 4 through IC10 to produce the 5 MHz 2CLK signal.

1.5.10 LOAD PULSE GENERATOR

Data retrieved from the Frame Buffer for display needs to be sent out to the CRT in a carefully coordinated manner. The load pulse circuitry generates the control signals which latch the data from the video memory at the precise moment so that a continuous stream of information is sent to the display. To set the display up for superimposing the background and window screens, two sets of load pulses must be generated which coincide with the MCYC periods of the ACRTC. These pulses need to be channelled so they arrive at the video shift registers at the proper time and in the correct sequence. Flip-flop IC9B uses AS and MCYC to signify that a valid address has been placed on the bus and controls timing pulses (generated by IC15C) through gate IC6B. Then IC15C combines 2CLK, MCYC and another timing pulse generated by IC10 to produce one load pulse every eighth dot clock into gates IC14 A and C.

To inhibit load pulses during cycles reserved for non-display periods, gates IC6D monitors both DRAW and HSYNC, turning gates IC14A and C off when those two signals are active. The last signal, MRD determines if offset load pulses for the superimpose window are produced by selectively turning on IC14A for regular load pulses or IC14C for load pulses which trail the regular loads by 8 dot clocks in the superimposed mode. Gates IC25C, IC16B and C and IC6C work with MODE_SELECT video attribute to channel regular loads for interleaved or offset loads for superimposed mode to the Video Pipeline.

1.5.11 SCROLL CHANNEL & PIPELINE CHANNEL

The video shift registers take parallel frame buffer display data off of the data bus and convert it into a serial stream of information for the CRT. There are two separate video channels, one used for the background screens which is designated to allow smooth horizontal pixel scrolling (Scroll Channel) and one is used for the superimposed window (Video Pipeline) which does not support smooth scrolling but can use either regular or offset load pulses to latch the video data off of the data bus.

The scroll channel uses regular load pulses which it uses to parallel load the frame buffer data into the first pair of scroll channel shift registers IC26 and IC27. On each following dot clock, the frame buffer data leaves the output of IC26 (least significant bit first) and shifts down one bit at a time into the second scroll channel shift register pair IC31 and IC32. After 16 dot clocks, 16 shifts have taken place, the second shift register pair are full and the first pair are empty. A new load pulse is generated and IC26 and IC27 are filled with the next Data word.

The current background screen's start dot address is placed on the video attribute HDS0-3 lines at the start of each raster scan line to determine which one bit out of the possible 16 will begin that current display line. The HDS lines control gates IC25E, and multiplexers IC33 and IC34 to determine which corresponding output line of the second shift register display video will be taken from. New data is continually shifted into this bit position from above and fed into Video Mixer IC17A via the multiplexers. For example, if the HDS lines indicated that the display should start with the 10th bit of the data word, the shift register output line for that bit would be selected by the multiplexers to be outputted to the video mixers, and on each new dot clock the next bit would be fed to this position. The 9 bits below bit 10 are ignored and not displayed. By updating the start dot address, a new starting bit position is selected and the display appears to move smoothly across the screen.

The video pipeline can either be loaded with regular load pulses to provide non-scrolling, non-superimposed display of video data, or with offset load pulses for latching the window during its cycle in the superimposed display mode. For each video channel there is separate control in any display mode to selectively enable or disable background or window or both screens.

1.5.12 VIDEO CONTROL

The video output sends the serialized display information to the CRT during the active video period. Video mixer IC17A combines the video pipeline and scroll channel data streams sending the result into gate IC7A. Whether the mixed video signal gets sent to the CRT depends on the control signal from IC12D which monitors the DISP 1 and 2 signals from the ACRTC and inhibits the video output if the system is not in the active video cycle. Gates IC16A and IC12C select whether a regular white on black display format or inverse video black on white is chosen, this is controlled by a video attribute.

1.5.13 Test Points

Monitor the following points with an oscilloscope to verify proper operation:

SIGNAL NAME	SIG. DESCRIPTION	TEST POINTS
2CLK	5 MHz	U11-1; U1-53; U11-9; U15-10
MCYC	2.5 MHz	U11-2; U1-56; U15-9
MCYC (INVERTED)	2.5 MHz	U24-4
HSYNC	30.3 KHz	U25-8; U11-10
HSYNC (INVERTED)	30.3 KHz	U6-12
VSYNC	57Hz	U25-12
DOTCLOCK	20 MHz	U31-8; U32-8; U26-7; U27-7; U29-7; U30-7;
DISP1	BACKGROUND SCREEN	U12-2 TIME 30.3 KHz
DISP2	WINDOW SCREEN	U12-13 TIME 30.3 KHz
DISP1+2	DISP1 and DISP2	U7-9 30.3 KHz
AS	ADDRESS STROBE 2.5 MHz	U13-1; U13-9; U13-3; U14-5; U9-10; U9-9
AS(INVERTED)	2.5 MHz	U2-11; U3-11
MRD	VERIFY TRANSITIONS APPEAR	U16-12; U14-1
WE	VERIFY TRANSITIONS	PIN 27 OF ALL RAMS (U18-U23)
DRAW	VERIFY TRANSITIONS	U6-13; U16-13
MAD 0-17	VERIFY TRANSITIONS	U2 AND U3 INPUTS AND OUTPUTS
CS LINES	CHIP SELECTS	U18-U23 PIN 20 U38-U39 PIN 20
LOAD	2.5 MHz	U14-13; U14-9
SCROLL LOAD	1.25 MHz	U26-15; U27-15
PIPELINE LOAD	1.25 MHz	U29-15; U30-15
PIPELINE VIDEO	VERIFY TRANSITIONS	U17-13
SCROLL VIDEO	VERIFY TRANSITIONS	U17-1; U17-2
VIDEO OUTPUT	VERIFY TRANSITIONS	U7-8

1.6 CO_2 Front End # 2418 (2409), # 2421 (2407)

1.6.1 Introduction

The capnometer interface system designed by Cascadia Technologies Corporation is the interface between the infra-red CO_2 Sensor (Capnostat™ Sensor) and the host microcomputer. It is made up of two (2) boards; the 2421 (previously 2407) digital front end board and the 2418 (previously 2409) analog piggyback board. They are interconnected through connector P3 and are connected to external circuitry through P208. These two boards provide continuous real time CO_2 reading to the host microcomputer through a serial link as well as providing all the necessary control signals to the Capnostat™ infra-red CO_2 sensor.

DIGITAL FRONT END BOARD #2421 (previously 2407)

1.6.2 Mode 1 Operation

The digital front end board provides the interface to the host microprocessor system as well as the control and timing of the analog interface to the CO_2 Sensor. It is operated by the Hitachi HD63701 microcontroller. This microcontroller is set up to operate in Mode 1 which functions as follows:

After the microcontroller is reset, the configuration of the device is determined by the state of three pins; P20, P21, and P22. These pins are latched into the program control bits when the reset goes high. This sets the microcontroller to Mode 1 which is called "Expanded Non-multiplexed Mode".

In Mode 1, port 3 (pins P30-P37) functions as the data bus bits D0-D7, port 1 (pins P10-P17) functions as address lines A0-A7, and port 4 (P40-P47) is configured as address lines A8-A15. Pin SC1 on port 3 is unused and pin SC2 acts as a R/W signal. Finally, port 2 (P20-P24) is configured as a combination I/O and serial communications port. P22 is configured as a 4800 Hz clock output, P21 is configured as a TTL level input which monitors XDUCER DISC, a signal which is generated when the CO_2 sensor opens. Pin P20 is configured as DTR which is a handshaking line of the serial communications to the host processor. Pins P23 and P24 are the RXD and TXD (receive data and transmit data) of the serial link.

1.6.3 System clocks

The crystal frequency input to the HD63701 is 2.4576 MHz, this frequency is divided by 4 to provide the system clock output on the E pin of the HD63701 and is also divided by 512 to establish the 4800 Hz clock out on P22. This 4800 Hz is ultimately divided down further (on piggyback board which will be explained later) to generate the AZ (Auto Zero) and S/H (Sample and Hold) signals which are the two main pulses that control acquisition of CO_2 data.

1.6.4 Mode configuration support hardware

In order to correctly write to pins P20-P22 on the HD63701 so it is configured to operate in mode 1 on power up, and then switch pins P20-P22 to I/O function lines, a Motorola MC14053 analog multiplexer/demultiplexer (IC1) is used. On system reset an

output from octal D-type flip flop IC3 is cleared which forces the A, B, C inputs of IC1 to zero. This internally switches the logic levels on XO, YO, and ZO inputs (001 respectively) to the X, Y, and Z pins of IC1, which are connected to pins P20-P22 on the HD63701. On the rising edge of the reset pulse the 001 levels are loaded into the program control register and establishes the processor mode (mode 1). Once the processor mode is established, a write to octal flip flop IC3 is done by software which sets the A, B, and C pins on IC1 to a high state. This switches pins X, Y, and Z to X1, Y1, and Z1 on IC1, that is DTR1, XDUCER DISC, and 4800 Hz clock are now connected to P20-P22 (they act as the I/O lines).

1.6.5 RD and WR signals

Additional microprocessor control signals RD and WR are further generated by gating the E pin on the HD63701 with SC2. The E pin acts as the system clock output and SC2 is R/W. The 74HC00 (IC17) along with SC2 and E generate the RD and WR (both active low) signals.

1.6.6 Decoding

Decoding on board is a memory map which consists of 8 blocks of 8 Kilobytes each. This is done by feeding A13-A15 into IC4 (74HC138) which is a 3 to 8 line decoder. The memory map output is as follows:

HEX ADDRESS	CHIP SELECT SIGNAL
0000-1FFF H	Unused
2000-3FFF H	Unused
4000-5FFF H	Unused
6000-7FFF H	IC3 chip select (octal FF)
8000-9FFF H	IC9 chip select (AGC latch)
A000-BFFF H	IC5 chip select (quad A/D)
C000-DFFF H	IC31 chip select (RAM) (not used)
E000-FFFF H	IC6 chip select (EPROM)

1.6.7 Memory

On board memory includes EPROM IC6 which is a HN27C64 (8K X 8), RAM IC31 a HM6264 (8K X 8) (this is a spare allocation on the board, it is not currently used), 128 bytes of RAM which is internal to the HD63701 microcontroller. There is 4 K bytes of PROM found internal to the HD63701 which are not used when in Mode 1 operation.

1.6.8 Octal flip flop IC3

The octal flip flop IC3 (74HC273) is used to generate a variety of signals. As already mentioned the CLR input pin on IC3 is connected to the reset system. This causes the outputs of IC3 to be cleared to 0 on each reset of the system.

The outputs of the flip flop are labelled Q1-Q8 and function as follows:

- Output Q1 controls the switching of IC1 which is used to set the HD63701 microcontroller (IC2) to mode 1 as described earlier.

- Output Q2 is a signal called DSR1 (Data Set Ready 1), this is a handshaking signal used in the serial communication link to the host microprocessor. It tells the host microprocessor that the interface system microcontroller is ready to receive serially transmitted data.
- Output Q3 is presently unused.
- Output Q4 is the HEATER CONTROL 1, it is a software heater control option for controlling the maintenance heaters in the CO_2 sensor. It is operational only if jumper W1 is installed on the analog piggyback board. With this option, software can override the servo-control thermistor amplifier circuit which controls the maintenance heaters by shutting down transistor Q2. At the present time this option is not used.
- Output Q5 is called HEATER CONTROL 2, this output directly controls transistor Q1 which is an IRF523 power MOSFET. This MOSFET switches the boost heater on or off.
- Output Q6 is connected to LED CR2, which flashes when the Cascadia system is running and is used as a method of determining if the system is functional after power-up.
- Outputs Q7 and Q8 are spare outputs and are not used.

1.6.9 A/D converter

The AD7582KN (IC5) is a four input channel successive approximation 12 bit CMOS A/D converter. Each input channel has an output range of 0-5 VDC. It is a medium speed converter with a conversion time of approximately 100 µsec per channel. Conversion results are read in 2 bytes, 8 LSBs and 4 MSBs. Either byte can be read first by the microcontroller.

The four analog channels which are input to the converter are DATACH, REFCH, TEMPCH1, and CURRENT. DATACH and REFCH are the direct outputs from the LF398 sample and hold circuits on the analog piggyback board. TEMPCH1 is the output of the thermistor amplifier circuit which is the servo-controlling circuit for the maintenance heaters in the CO_2 sensor as mentioned earlier. CURRENT is an input which represents the voltage drop across a resistor (R60) on the piggyback board. This resistor is in series with the infra-red source in the CO_2 sensor. By monitoring the voltage across the resistor, the current to the source can be monitored to protect against malfunctions.

1.6.10 AGC circuit

The AGC (Automatic Gain Control) circuit is made up of IC9, IC13, and IC14. The 74HC273 (IC9) is an octal flip flop and IC13 and IC14 are CD4067 CMOS analog multiplexers/demultiplexers. On each of the 16 outputs on IC13 and IC14 is a 1% resistor to ground. The resistors are slightly different in value, ranging from 1.96 KΩ to 12.1 KΩ. During calibration of the sensor (after warm-up) the octal flip flop IC9 is used to control which resistors are internally selected by IC13 and IC14. The selected resistors are connected through to lines DGAIN and RGAIN which connect over to the piggyback board and set the gains on the IC28 OPAMP circuits of the DATA and REF channels.

1.6.11 Voltage reference

VREF is a +5 V signal which is used throughout both the digital front end board and the analog piggyback board. VREF is generated by a precision voltage reference (IC8). On the digital front end board it serves as the reference voltage for the A/D converter, and is fed to IC19, an emitter follower circuit to generate VB, a bias voltage used in the CO_2 sensor. Further uses on the analog piggyback board will be explained later.

1.6.12 Main heater control circuit (only on 2421 boards)

The MAIN HEATER CONTROL line provides the required power for both the boost heater and maintenance heaters in the CO_2 sensor. It includes the circuitry of IC30 pins 1, 2, and 3, transistor Q19, and Q20. Different safety features are built into this circuitry for safe sensor use. For example, the XDUCER DISC signal can be generated 2 ways:

- by unplugging the sensor,
- if the thermistor in the CO_2 sensor should open.

In either case the XDUCER DISC signal is fed directly to Q20 which shuts down the gate voltage to Q19. This cuts off power to the maintenance heater control output.

In addition to this, the output from the thermistor amplifier circuit TEMPCH1 is fed directly to IC30 pin 2. This circuit is a comparator circuit which compares the output TEMPCH1 to a 6.7 VDC level provided by the resistor divider of R140 and R141. Should any circuitry malfunction and cause thermal runaway, the overheating of the sensor causes TEMPCH1 to exceed 6.7 volts and power is again disconnected from the MAIN HEATER CONTROL line by shutting off Q19.

ANALOG PIGGYBACK BOARD #2418 (previously 2409)

1.6.13 Introduction

The analog piggyback board provides the required interface circuitry for data acquisition from the CO_2 sensor. All required power and biasing voltages to the infra-red source and detectors is done through this circuitry. Before going into the circuitry, it is best to give a brief overall explanation of how the CO_2 data is acquired.

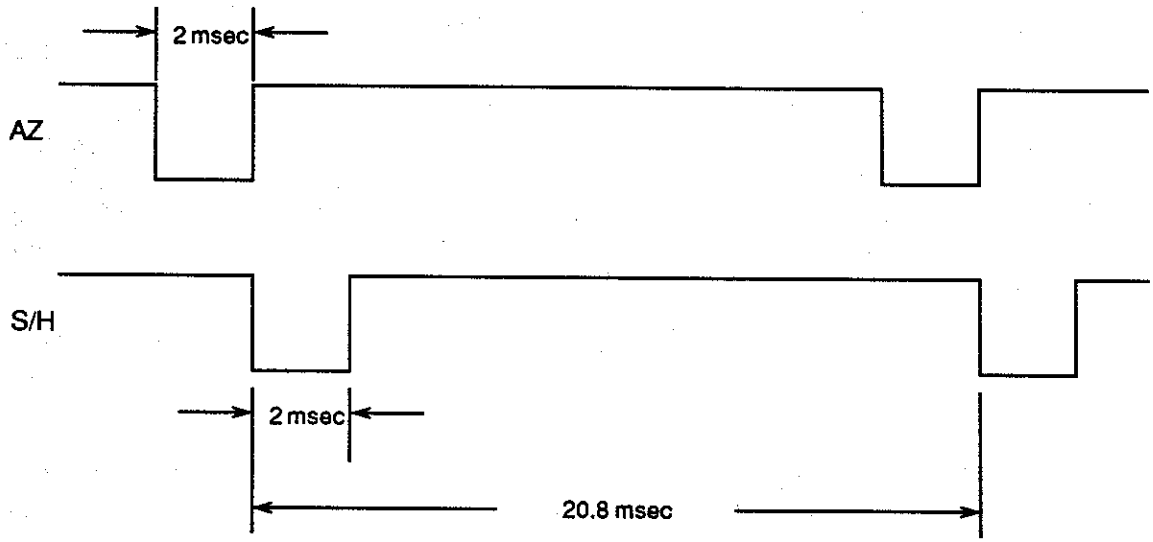
As the CO_2 passes through the airway adaptor, an infra-red source is pulsed at a rate of 48 Hz. The infra-red energy from the source is absorbed partially by the CO_2 in the airway and then passes through two light filters, one filter within the infra-red frequency spectrum of CO_2 absorption and one outside the infra-red frequency spectrum of CO_2 absorption. Behind each light filter is an infra-red detector. The detector behind the filter within the CO_2 absorption range is for the data channel and the detector behind the filter outside the CO_2 absorption range is for the reference channel.

To acquire a precise level of CO_2, both channels are sampled simultaneously and the level of CO_2 is determined from the ratio of the data and reference channels. The ratio is compared to a lookup table in memory to establish the correct value in units of mmHg.

1.6.14 AZ (Auto Zero) and SH (Sample/Hold) pulses

The combination of IC10, IC11, and IC12 provides the timing pulses called AZ and S/H. Both signals are active low pulses of about 2 msec every 20.8 msec. This is equal to 48 Hz which is the sampling rate of the system.

The method by which these pulses are generated is by dividing down the 4800 Hz clock output signal from the HD63701 on the digital front end board. The 4800 Hz signal is brought across on connector P3-14 and is run directly into IC12 which is a CD4017 decade counter. This divides the signal by 10 to produce a 480 Hz signal. The 480 Hz signal is then run into the clock input of IC11 which is a CD4018 presettable divide by N counter. This counter is set up with the Q4 output tied to the data input so that 48 Hz is attained on all outputs Q0 through Q4. These outputs all have a 50% duty cycle. By connecting these outputs to the inputs of IC10 which is a 74HC138 3 to 8 line decoder, the S/H and AZ pulses are produced with the required pulse width of 2 msec on a time base of 40 Hz. The pulses occur such that the S/H pulse is generated immediately on the rising edge at the end of the AZ pulse. This is shown on the following timing diagram:



1.6.15 Acquisition of CO_2 data

The waveforms described in 1.6.14 are inverted by IC20 to produce active high pulses. The active high AZ and S/H pulses are the two pulses by which CO_2 data is collected. This is done as follows:

The data acquisition cycle begins with the AZ pulse which is connected to the gate of FETs Q11 and Q16. These FETs are connected to the inputs of IC15 and IC16 which are the LF398 Sample/Hold amplifiers of the Data and Reference channels. The AZ pulse turns on Q11 and Q16 which short the inputs of the Sample/Hold amps to ground providing a true zero discharged level on both of the channels before new data is acquired.

The AZ pulse is also fed through C53 which is a 1µF capacitor. This capacitor in combination with diodes CR8, CR9, and CR10 provide a differentiated pulse from -4 V to 0 V at the gates of FETs Q10 and Q15 which are inputs to the detector biasing circuits driven by IC27. Both the DATA and REF channel circuitry that set the bias voltages on the

detectors are identical. For the most part, only the DATA channel circuitry will be discussed to avoid redundancy.

During the AZ pulse, no SOURCE pulse is driving the infra-red source. It is at this point that Q10 and Q15 are turned on and zero source bias level is set on the detectors for the DATA and REF channels. The RC combination of C50 and R72 (on the DATA channel) have a high time constant of approximately 0.26 seconds. The zero source current level of DATAOUT is fed through Q10 on the AZ pulse and this in turn biases the transistor circuitry of Q7, Q8, and Q9. Transistor Q7 acts as a current source from +15 V through a 10 KΩ resistor (R70) and along with output of IC27 controls the biasing point of Q7 and Q8. VBDATA is the bias voltage for the DATA channel detector and when properly set should be in the -30 to -40 VDC range. It is at this point that DATAOUT should be zero volts.

Immediately following the AZ pulse is the S/H pulse. This pulse is active low coming out of IC10. It is connected to a variety of circuits which control the actual CO_2 data level acquisition.

The S/H signal is routed to IC29 pin 2. This is the input to a pulse width watchdog circuit. This circuit is to protect the infra-red source from overheating due to a circuitry lockup with the S/H pulse actively driving the infra-red source. If this situation were to occur, IC29 pin 7 would go to a low state and the initial source drive switch output Q6 would be disabled which in turn would disable the source drive circuitry.

The S/H pulse is differentiated through C38 and then drives the gate of Q6. This turns Q6 on and off to provide the initial stage of the source drive timing pulse circuitry. This pulse is first run through the emitter follower circuit IC24 pins 5, 6, and 7. On the output pin 7 is a signal of 2.5 V with an active low pulse to 0 V. The two resistors R54 and R55 are tied from this output to -15 V. These resistors form a voltage divider which provides a pulse from +0.57 V to -1.66 V on the high impedance input of IC25. The circuit of IC25 is a non-inverting amplifier with a gain of 9, providing the source drive of -15 V to +5 V.

The source drive signal at this point is run through a one ohm resistor (R60) and then is sent directly off board to the source on P3-7. The resistor R60 provides a small voltage drop in order to measure the source current. To do this, the output IC25-3 is fed into inverting amplifier U26-1,2, and 3 which has a gain of -0.5 V. Output U26-1 is fed into inverting summing amplifier IC26 pins 5, 6, and 7 with a gain of -20 through the input of R63. This gives a total gain of 10 (-0.5 x -20) through this side of the summing amplifier. The other input of the summing amplifier is connected to the source drive after it has passed through the one ohm resistor R60. It has a gain of -10. When there is no current being driven through the source (IC25-3 = -15 V), the output U26-7 has a zero volt level. When the source is being driven (IC25-3=+5V), the slight voltage drop across R60 is seen on IC26-7. This current output goes directly off board on P3-9 to the digital front end board and is fed into the A/D converter IC5.

Besides being the pulse which generates the source current drive, the S/H pulse is inverted through IC20 to provide an active high pulse. This pulse is fed through P3-18 to the digital front end board and is connected to the NMI input pin of the HD63701 microcontroller. This signals the controller to start the CO_2 data acquisition software routines. Finally, the active high S/H pulse is connected to pin 8 of the sample/hold amplifier IC15 and IC16 to control the sampling of the DATAOUT and REFOUT channels.

1.6.16 Additional Protection Circuitry

ICX1 is a MAX8211 undervoltage protection circuit designed to trigger when Vcc reaches 4.75 VDC or less. It disables the output of the initial source drive switch Q6. This is found only on the 2418 boards.

Transistor Q18 is a VP080M FET which switches +15 V to source drive amplifier IC25 pin 4. The circuit is set up so that if the +15 V or -15 V supply is lost, the source drive circuit will shut down.

Transistor Q5 is a J270 FET whose gate is connected off board to the power "on" latch of the 2401 board. This disables the source drive immediately on power "off" to prevent any harmful glitches from damaging the infra-red source.

The combination of C73 and R78 provide a protection circuit to the infra-red source from random pulses during power up. The time constant of the RC circuit does not allow IC10 to be enabled until long after the +5 V Vcc line has become stable.

Transistor Q3 is a 2N5551 NPN which shuts down the -80 V regulator circuitry when XDUCER DISC becomes active. This eliminates the high bias voltages when the transducer is unplugged from the unit or if the thermistor fails in the open state.

1.6.17 -80 Volt supply

As described earlier, -80 volts is used in the biasing of the DATA and REF channel detectors. This -80 VDC is generated by the combination of circuits IC22, IC23 -1, 2, 3, and transformer T1. First, IC23 is a 100 K Hz oscillator which drives Q17, Q17 in turn, switches current to transformer T1. Capacitor C36 provides the differentiation on the input of T1 to cause the polarity reversal. On the output of T1 is diode CR5, this is a 1N4938 which rectifies the transformer output to only pass negative polarity. The rectified signal is fed back through R46 to the two stages of IC22. These two stages are the regulator section which controls the turn on of Q4, the FET which switches power to transformer T1.

1.6.18 XDUCER DISC

As mentioned earlier, XDUCER DISC is a signal which is generated when the transducer is unplugged or if the thermistor in the infra-red sensor becomes open. The circuit is the LM393 comparator circuit IC23 pins 5, 6, and 7. Resistor R30 and R31 form a voltage divider which generates a 0.75 V level at the (+) input pin 5. The T2 input is nominally 2.5 V with the sensor plugged into the unit and warmed up. Should the sensor become unplugged or the thermistor in the infra-red sensor opens, the 2.5 V level drops to 0V which causes IC23 -7 (XDUCER DISC) to go high.

1.6.19 Temperature regulation circuit

In order to keep the windows in the airway from fogging due to moisture in the patients breath, a constant temperature of 43 degrees centigrade is maintained by the heaters in the infra-red sensor. These heaters are controlled by the temperature regulation circuits of IC21. The circuit of IC21 -1, 2, and 3 is a differential amplifier circuit whose non-inverting input varies with thermistor resistance. The thermistor resistance in the

sensor varies with temperature from approximately 10KΩ at 25°C to 5.11KΩ at 43° C. This produces a voltage of -5.28 V on IC21 pin 1 at 25 °C, and 3.43 V at 43 ° C.

The next stage IC21 5, 6, and 7 works in combination with CR11 and CR12 to perform a slightly different function from a straightforward differential amplifier. Diode CR11 and CR12 are both 1N270 germanium diodes, and when the system is at room temperature, these diodes clamp the inverting input IC21 -6 to -0.6 V. This causes IC21 -5, 6, and 7 to act like a comparator circuit, and since IC25 -5 is held at 3.5 V the output IC21 -7 is driven to the positive rail which drives heater control FET Q2 to fully on. As the sensor heats up and the voltage on IC21 -1 becomes greater than -0.6 V, the diodes CR11 and CR12 are reverse biased and no current flows through them. At this point, the second stages IC21 -5, 6, and 7 acts as a differential amplifier which drives Q2 with only enough current to maintain a sensor temperature of 43° C.

1.7 Saturation Front End # 2267, # 2268

1.7.1 Introduction

The SaO_2 Front end is currently a two board system with an analog piggy-back board connecting into the main digital board through a 40 pin connector. The majority of the circuitry on these boards is isolated from the units main power supply. The data from the SaO_2 Front End is sent serially to the main CPU of the Model 7000. The plethysmogram data is sent at a 50 Hz frequency (every 20 msec). On detection of a valid beat or on change in front end status the data rate is increased to 100 Hz by alternating plethysmogram data with saturation data, pulse rate data, and front end status data. After sending the status data the data rate is again reduced to 50 Hz until the next valid beat or change in status.

DIGITAL BOARD #2267

1.7.2 Non isolated circuitry

The non-isolated circuitry consists of a DC-DC converter and opto-isolators for interfacing with the rest of the front end. IC1 is an astable vibrator which is oscillating at 1.6 KHz. Its outputs are fed into IC2 along with the FE enable line. If the FE enable line is high the oscillations appear at the gates of Q1 and Q2, when the FE enable line is low both Q1 and Q2 are held low (off). The opto-isolators are dual, low current, high gain components allowing serial transmission, reception, and handshaking between the front end and the Model 7000 CPU.

1.7.3 Isolated power supplies

The raw AC isolated voltage coming from T1 is rectified by D1 and smoothed by capacitors C7, C8. A VDDI line is produced by IC5 which is capable of supplying 5 volts at 100mA maximum. IC6 produces a VLEDI line which is used exclusively for the sensor LEDs. Because of the relatively large currents turned on and off (≈60 mA) at the sensor leads this line requires further filtering via the LC network in an attempt to keep the drain on IC6 constant. The analog lines +VAI and -VAI are passed through RC filters (R3, C12 and R4, C13) to suppress digital and other types of noise. The analog lines are maintained at approximately +7.5 and -7.5 volts respectively.

1.7.4 Microprocessor and associated circuitry

The microprocessor used on this board is the NSC800 manufactured by National Semiconductor Corporation. On the schematic the NSC800 is identified as IC9, its data bus is multiplexed with the low order byte of the address bus. The lower byte of the address bus being demultiplexed by IC10 enabling a full 16 bit address bus. The NSC800 is run at 4 MHz using an 8 MHz crystal (Y2) and its associated circuitry R6, C18, C19. System reset circuitry is present at pin 33 on the NSC800, this consists of R7 and C31 which produces a slow transition from high to low which is long enough for the power supplies to stabilize, this is then inverted by IC18 (pin 2). When the RSTIN pin goes high the NSC800 will unlock from its reset condition and restart normal operation from the start address 0000. The following functions of the NSC800 are disabled by the tying of these lines high (via RP3).

INTR- The lowest priority interrupt
BUSRQ- Bus request from another device
WAIT- A delay line for slower peripherals
PS- The power save line, this is not used here.

All the interrupt lines are tied high - enabling them to be at a normally high state unless an interrupt is being actively requested by the interrupt circuitry (see section 1.7.7).

1.7.5 Memory and memory mapping

The NSC800 can support up to 64 Kilobytes of memory. This CPU system allows for up to 32 K of ROM and 8 K of RAM. The ROM (IC14) is selectable between an 8 K device (27C64) and a 32 K device (27C255) via the link LK1 (currently set to support the 8 K device). The RAM (IC16) is also selectable, LK2 allows support of either a 2 K device (6116) or an 8 K device (6264), currently the 2 K device is used. To allow a minimum of memory decoding the memory mapping is kept simple. The ROM is enabled if A15 is low and IO/M is low, the RAM is enabled if A15 is high and IO/M is low.

1.7.6 I/O decoding

The I/O address space for the front end is decoded by IC11 a 3 to 8 line decoder, thus a possible eight peripherals devices can be enabled from this device. The I/O decoding sits at the zero page address of the memory map and is distinguished from memory addresses by the IO/M line being high for I/O decode. The I/O devices used on the 7000 saturation front end sit at the following addresses:

ADDRESS	CIRCUIT REF.	I/O DEVICE
0080-0087	D4 pin 1	NMI watchdog circuit
0088-008F	IC11 (2268 board)	Gain DAC enable
0090-0097	IC12 (2268 board)	LED drive DAC enable
0098-009F	IC10 (2268 board)	ADC enable
00A0-00A7	IC19 pin 12	RSTC clear line
00A8-00AF	IC 9 (2268 board)	Offset DAC enable
00B0-00B7	IC7 pin 11	UART enable
00B8-00BF	----------	Not used

1.7.7 Interrupts and interrupt timing circuitry

NMI watchdog circuitry

The watchdog timer is an essential part of the circuitry indicating basically whether the NSC800 is still in control of the front end circuitry. The watchdog timer can be seen as the circuitry surrounding the device Q3. It functions by making sure that the watchdog line (address 0080 H) is pulled low by the software at least every 10 seconds. Thus if the software "crashes" and falls into a locked loop the watchdog line will not get accessed and will be pulled low.

If the watchdog line does not get pulled low within the specified period then the RC point (R9, C29) will reach a high enough voltage to turn the schmitt trigger low (IC18 pin 12) which will turn the FET (Q3) off enabling capacitor C30 to charge. When this reaches a high enough voltage, the schmitt trigger (IC18 pin 10) will be turned off (low) causing an NMI. The NMI resets the system and sets the NSC800 to start again at address 0000 H.

RSTA

The RSTA circuitry is designed to interrupt the NSC800 every 500 msec. It achieves this by dividing down the strobe line from the 2268 analog board. On RSTA the NSC800 reads the ADC which also clears the RSTA line. The RSTA interrupt is the major interrupt for the front end and it is the only time that the front end conditions are examined and changed.

RSTB

The RSTB line is used to detect when data is being sent from the 7000 CPU. When a received byte of data is available for the NSC800 to read, the UART sends a signal to the NSC800 which is received as a RSTB interrupt. Once the NSC800 reads the data in the UART the RSTB line is cleared.

RSTC

The RSTC circuitry is designed to interrupt the NSC800 every 250 msec. This is achieved by dividing the system clock (4 MHz) by 1,000,000 to produce a 4 Hz signal. On RSTC the NSC800 writes out to address 00A0 H which then clears the RSTC line. The RSTC is used in the system timing applications and averaging routines.

1.7.8 Serial communications

The serial communications between the front end and the 7000 CPU are asynchronous with handshaking. The communications protocol is 8 bits, no parity, one stop bit at speed of 19,200 baud. IC8 and its supporting circuitry Y1, R5, C15, C16, generate the required clock signal for the UART (IC7) to transmit and receive at this speed.

ANALOG BOARD #2268

1.7.9 Analog timing circuitry

The timing circuitry on the analog board provides the following signals:

1.) The red channel LED "on" time pulses.
2.) The infra-red channel LED "on" time pulses.
3.) The red channel sampling time pulses.
4.) The infra-red channel sampling time pulses.
5.) The strobe signal for RSTA.

The timing waveforms are explained below starting with the STAT waveform which all other waveforms are based upon. The numbers in [ ] correspond to the waveforms on the following page for identification.

[1] All timing originates from the STAT output of the eight channel ADC IC10 (pin 12) which is fed to inverter IC14 (pin 5).

[2] The output of the inverter IC14 (pin 6) is simply an inverted STAT waveform and is fed to a pulse width detector consisting of R55, D10, C58, and also goes to the clock input of IC17 (pin 8).

[3] This resembles the output of the pulse width detector IC14 (pin 3).

[4] The output of the pulse width detector is fed into inverter IC14 (pin 3) causing its output pin 4 to switch negative only when the input exceeds a threshold voltage of approximately 3 volts. The RC time constant produced by R55 and C58 will allow a 72 µsec pulse to reach this threshold voltage which is generated after a channel 1 conversion at the ADC IC10.

[5] The STAT output shown in [1] is also fed to a differentiating circuit consisting of C55, R54, D11. The output of the differentiating circuit triggers IC13 (pin 2) which is a monostable multivibrator.

[6] The output of the monostable has a pulse width which is determined by R53 and C56. It is a positive going pulse of 63 µsec ±10 µsec whose leading edge coincides with the falling edge of the STAT waveform [1].

[7] The waveform in [6] is fed to a delay circuit consisting of R56, D12, C59 whose output should appear as shown IC14 (pin 11).

[8] The output of inverter IC14 (pin 10) will only trigger when the input (pin 11) is above the threshold voltage of approximately 3 volts. This delays the leading edge of the pulse which is then inverted by IC14 (pin 8).

[9] The monostable output IC13 (pin 3) is inverted by IC14 (pins 1 and 2). This is fed to IC15 (pin 10).

[10] IC15 is configured as a latch, the other input to this latch comes from IC14 (pin 4) whose waveform is shown in [4]. The output of the latch is fed to IC17, an 8 bit shift register clocked by the inverted STAT line shown in [2]. The latch out-

put also produces the STROBE timing waveform which is used to generate the RSTA interrupt every 5 msec. This waveform shown is the STROBE line.

[11] The ANDed output of IC16 (pin 8) is the red LED "on" time (TP25).

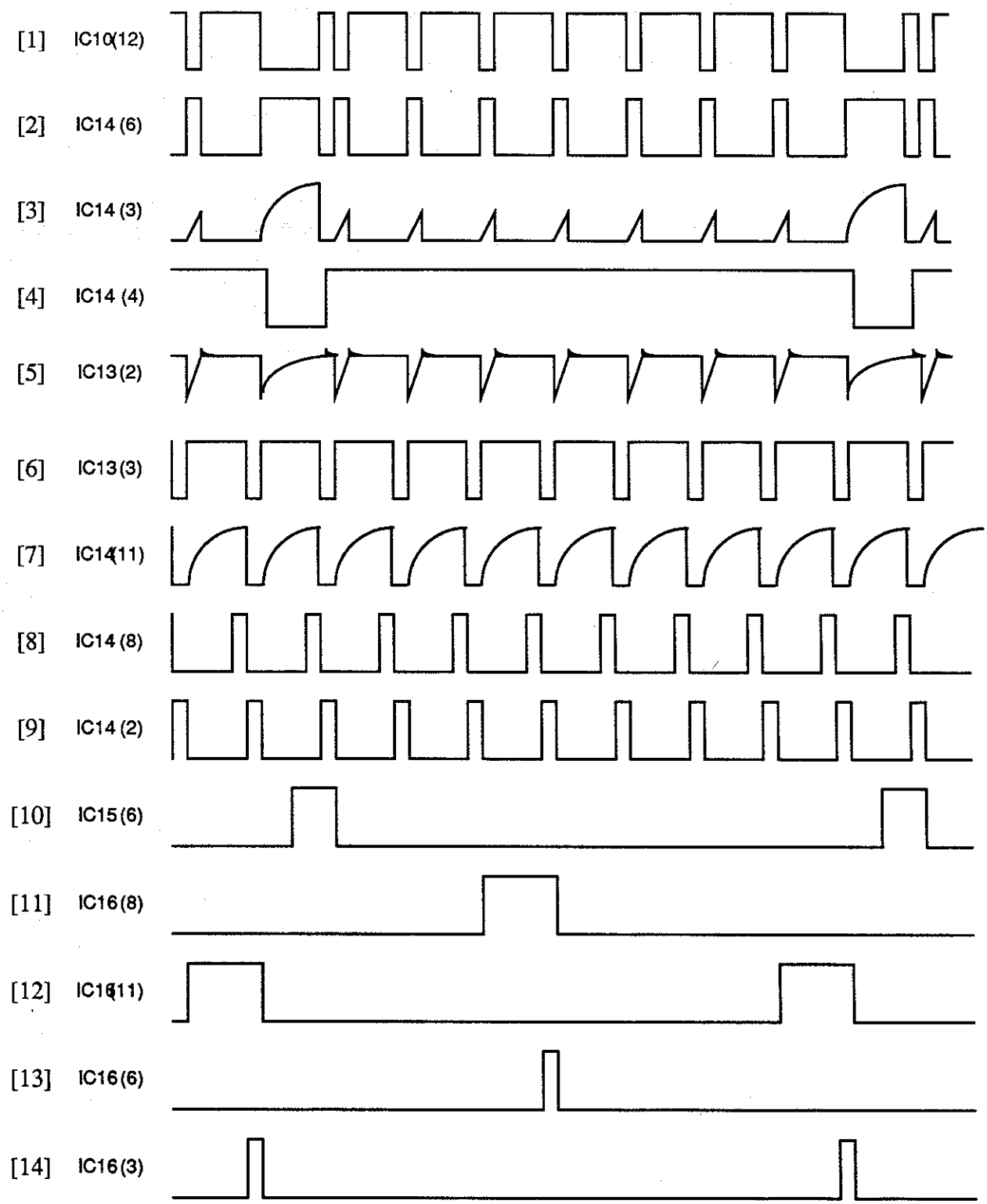
[12] The ANDed output of IC16 (pin 11) is the infra-red LED "on" time (TP26).

[13] The ANDed output of IC16 (pin 6) is the red LED sample time (TP24).

[14] The ANDed output of IC16 (pin 3) is the infra-red LED sample time (TP23).

NOTE: For both the red and the infra-red channels the LED is turned "on" before the sample gate. This short delay allows the photodiode return path circuitry to settle before the sample data is taken. Both the LEDs and sample gates are turned "off" at the same time.

Timing waveforms for SaO_2 board:



1.7.10 Vref circuitry

An on board voltage reference is generated for use by the A/D and D/A converters on the front end. A constant voltage of -1.23 VDC is generated from IC18 and D1, this is then amplified by non inverting amplifier IC1 (output pin 1) configured for a gain of 2.02 through R1 and R2. The resulting output is Vref which is -2.5 VDC.

1.7.11 The A/D converter

The analog to digital conversion is performed by IC10, an 8 channel 8 bit converter (AD7581). It is clocked at 1 MHz from the divided down NSC800 clock. The device automatically cycles sequentially through each analog channel from channel 7 through to channel 0, then repeating the process again from channel 7. The results from each conversion are stored in a dual port RAM. The device takes 80 µsec per conversion so each channel is sampled every 640 µsec. At the end of each conversion the STAT line outputs an 8 µsec negative pulse, which is extended to 72 µsec at the end of channel 0 conversion.

During the 5 msec RSTA interrupt all the used channels are read from their relevant RAM locations. The ADC is selected from the I/O decoder and the appropriate channel selected from the address lines A0, A1, A2. The converter uses the -2.5 V as its reference input and the BOFS pin is used to set the device into bipolar operation.

1.7.12 LED drive circuitry

The red and infra-red drive channels work identically, therefore only one channel (red LED) need be described (component references between the two are different, the infra-red channel equivalents will be listed in [ ]). The LED drive current is controlled by a dual DAC (AD7528) IC12 and buffer amplifier IC7 (pin 1) [IC7 (pin 14)]. The output follows the following equation:

$$\text{Vout} = (n * (- \text{Vref})) / \text{resolution of DAC}$$

n = digital setting of the DAC (0 - 255)
Vref = input reference voltage (-2.5 V)
resolution of the DAC = 8 bits which corresponds to 255, therefore the limits are;

$$\text{Vout} = (0 * (-2.5)) / 0 = 0 \text{ V}$$

or

$$\text{Vout} = (255 * (-2.5)) / 255 = 2.5 \text{ V}$$

This output voltage is switched "on" and "off" by the analog switch IC8 (pins 10 and 11) [IC8 (pins 8,9)] which is controlled by the timing circuitry described in section 1.6.9. After the switch the voltage passes through a voltage divider consisting of R47 and R49 [R48, R50] then passes through buffer IC7 (pin 7) [IC7 (pin 8)] . The output of this buffer controls drive transistor Q1 [Q2], which is configured as an emitter follower whose collector is connected to the cathode of the sensor LED (the anode of the sensor LEDs are

connected to VLEDI). The voltage at the base of the transistor along with the emitter resistance R51 [R52] control the amount of current through the transistor hence the current through the LED. The amount of current through the LED determines its brightness.

1.7.13 Offset circuitry

The offset circuitry verifies that the ADC reads in bipolar mode with 0 V sitting at value 0080 H which is the halfway point for the converter. The voltage at the BOFS is examined at the count of 0080 H and compared to channel 6 input of IC10 (AD7581) which is at ground potential.

1.7.14 Analog signal input from the photodiode

The input from the photodiode is connected between pin 12 and 13 on IC5 which is a differential amplifier configured as a current to voltage converter. The output from this appears as a double train of pulses representing the red and infra-red signals. The amount of light received at the photodiode is dependent upon the amount of light absorbed by the tissue in the path of the LEDs. If placed over a well perfused site the pulse heights will vary with the amount of blood at the site which changes as cardiac output changes.

The output of the differential amplifier is fed into a four pole high pass filter consisting of IC5 (outputs pins 7,8). This removes the DC and unwanted 50/60 Hz ambient light interference. The high pass filter introduces an offset which is corrected by a half wave rectifier. The output of the rectifier has a zener clamp to prevent the signal from exceeding 5 V. The amplifier IC4 (output pin 1) preceding the sample and hold circuitry simply inverts the signal to a positive going polarity.

1.7.15 Signal splitting

The pulses from IC4 pin 1 are fed into switches on IC8 which demultiplex the red and infra-red signals. This is done by turning the red LED channels switch "on" when the red channels pulse is present and keeping it off at all other times. This way the sample and hold for the red channel only sees red LED pulses. The same occurs for the infra-red channel. The value of the pulses are held constant by the low leakage holding capacitors in the sample and hold circuitry C35, C36. When the switch is turned "on" the capacitor charges to the sample voltage, when the switch closes there is no discharge path for the capacitor so it retains its voltage. This voltage is then reproduced at the output of buffers IC3 (the high input impedance of the buffers prevents the discharge of the capacitors through them).

1.7.16 The DC path

The outputs from the sample and hold buffers are fed into summing amplifiers where they are summed with the reference voltage Vref. This is done to achieve full range of the ADC which follows this circuitry. The capacitors C30 [C29] are to reduce any AC component of the signals.

1.7.17 The AC path

The output from the sample and hold buffer is also AC coupled by C34 [C33] to allow only the time varying component of the signal to pass. This signal is then amplified by 20 (only 5 for the infra-red channel) by IC3 (pin 8) [IC3 (pin 7)]. This is fed into a dual DAC IC11 which is configured as an attenuator. The amount of attenuation is controlled by software and is done to achieve the best size AC signal for the ADC without exceeding its limits. The attenuator output is buffered by IC6 before being AC coupled by C47. The signal is then amplifies 100 times by IC2 before being sent through a low pass filter IC6. The output of the low pass filter is then sampled on the channel 2 input on the ADC.

1.7.18 Noise checking circuitry

The ADC has two channels available for noise detection on the front end. The first (channel 0) examines the output of the first stage of the front end. This is done by summing the first stage output with Vref and reducing the AC component by C37. Thus the sum of the DC and the pulse height are examined at this stage. The second channel (channel 7) examines the input to the sample and hold circuits when the pulse is not present to see if the AC component is greater than a pre determined setting.

1.7.19 Ear probe detection circuitry

The detection of an ear probe is determined by IC15 (input pins 12,13) and R57. With no earprobe the input to the schmitt trigger is held high by R57, with the presence of an earprobe this input is brought low which signals the UART on the digital board through the PBEDET line.

1.8 Motherboard, CRT Assembly, and Front Panel

1.8.1 Motherboard

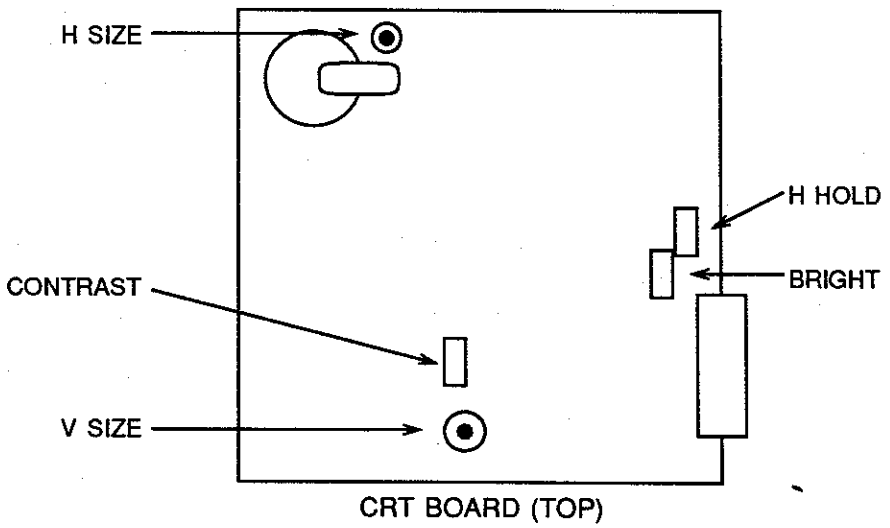
The Motherboard houses all of the other circuit boards that constitute the Model 7000 system. All communication between the microprocessor and the elements it supports (video controller, front end boards, etc.) is run through the Motherboard. The three digital card slot connectors are interchangeable, the same holds for the front end board card slots.

The AC INPUT/RAW DC block as described in the Power Supply Board theory of operation is situated on this board. The output of the transformer is connected to J212, it is then rectified and filtered by bridge rectifier D1 and capacitors C1 and C2. The output voltage from here is regulated by an LM317K which is mounted on the rear panel of the unit, it's three terminals plug into J217 on the Motherboard. Resistors R1 and R2 along with VR1 control the output voltage from the regulator. This output should be +14.5 V ± .002 V with no load. Diode D2 protects the regulator from reverse polarity which is possible while operating under battery power.

1.8.2 CRT Assembly

The CRT assembly which consists of the CRT and the CRT board is the COMPUTRON 115DMX with a 7" display. It receives its power from the RAW DC line of the

power supply which it shares with the fan. The CRT board is situated on the Motherboard and receives all of its signals from J213. The CRT is fastened to the front panel assembly by four screws. There is a ground cable, high voltage line, a four wire connector, and an eight wire connector which interconnects the CRT to the CRT board. Most of the adjustments for the CRT are located on the CRT board (the focus and magnets are on the CRT).



NOTE: consult Adjustment Procedure for H HOLD control.

1.8.3 Front Panel

The Front Panel holds the membrane switch key panel which enables the user to operate the monitor. All the switches and indicator LEDs from the membrane keypanel are connected to the Motherboard by a ribbon cable at J214. The Cal Cell is Attached to the front panel and is used in calibrating the Capnostat™ CO2 sensor. The switches associated with the Cal Cell are plugged into J215 on the Motherboard. Connector J216 from the Motherboard is for the Capnostat™ sensor jack, the SaO2 sensor jack plugs directly into the 2268 SaO2 Analog board.

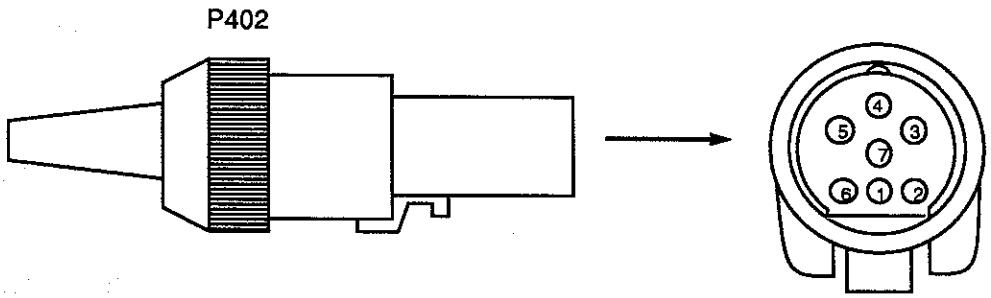
1.9 SaO2 Sensors

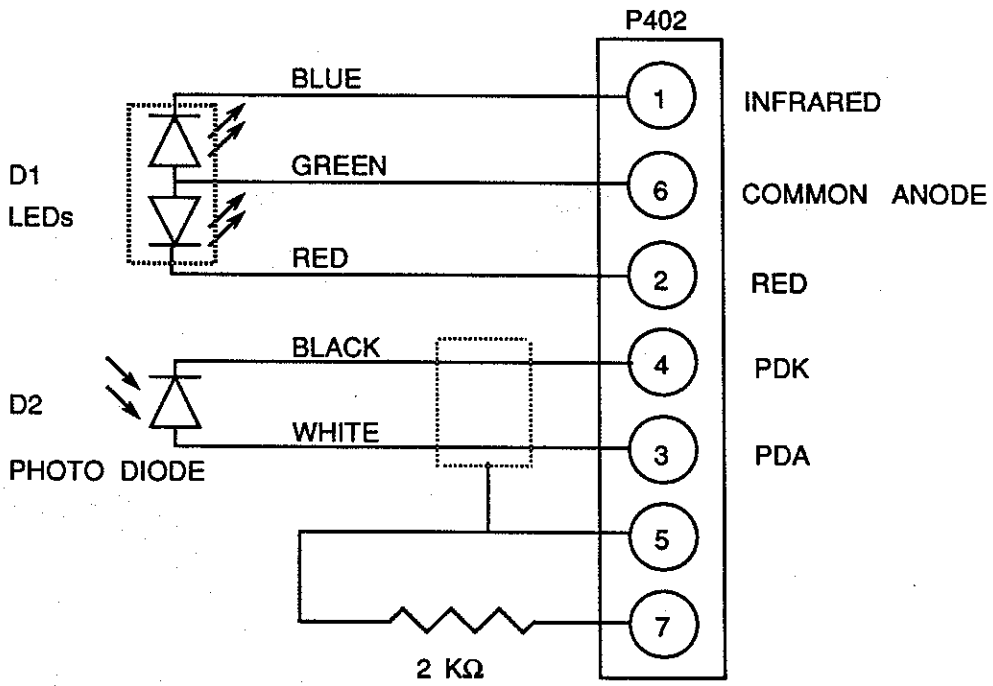
1.9.1 General

There are three types of SaO2 sensors available for use with earlier Model 7000 (identified by a green SaO2 input connector). The three sensor types are, ear, finger, and Re-Flex™. Refer to the Operating Manual for details on patient application of the various sensors. Current production models incorporate the SuperBright™ sensors and are not compatible with earlier models. An error message will be displayed if the wrong style probe is used.

1.9.2 Sensor part numbers and schematic

The figure shows the sensor cable connector, P402. The rear view shows the pinouts for the connector, the connector and cable assemblies are identical for each of the different types of sensors. The schematic is a representation of the circuitry found in each of the three sensors, the mechanical packaging is the only difference.





NOTE: Resistor is fitted on Ear Sensor only.

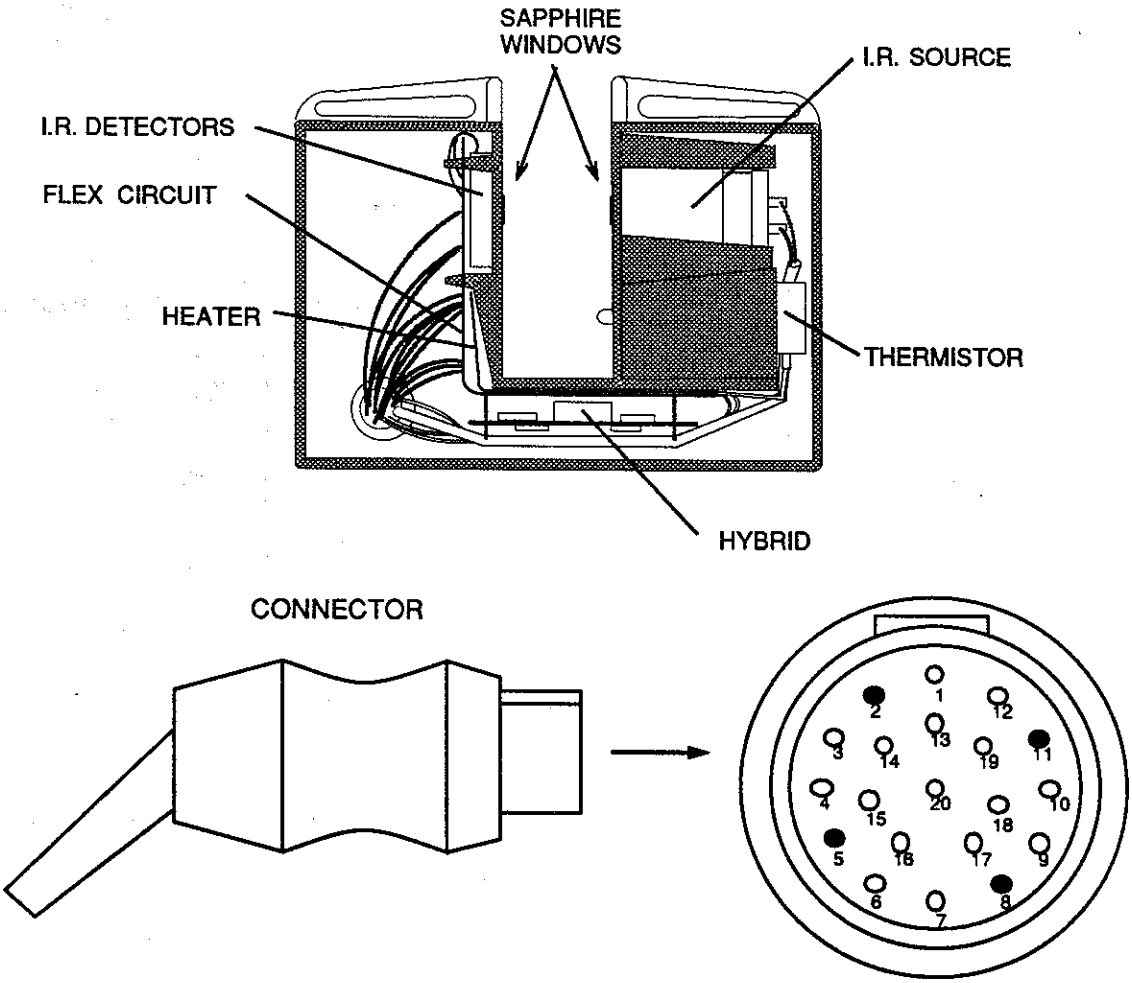
1.10 CO_2 Sensor

1.10.1 General

The Novametrix Capnostat™ Sensor which is used to monitor CO_2 levels contains sophisticated circuitry which is housed inside a gas tight plastic case. For this reason should any malfunction or damage occur with a sensor replace it and do not attempt repair. Contact Novametrix Service Dept. for replacement or problem sensors

1.10.2 Sensor part numbers and schematics

The following figure shows a representation of the inside configuration of the Capnostat™ sensor:



PIN#	DESCRIPTION
1	Source (black, thin)
2	Spare
3	Vb ref (blue)
4	Ref out (green)
5	Spare
6	Data out (orange)
7	Vb data (clear)
8	Spare
9	Heater (white, thick)
10	Outside shield
11	Spare
12	-15 V (white, thin)
13	Source shield
14	Vb (light brown)
15	T2 (violet)
16	+5V (red)
17	Boost (black, thick)
18	-15V (yellow)
19	+15VB (brown)
20	Analog ground (gray)

The following is a list of sensor related parts and part numbers.

PART#	DESCRIPTION
4981	Capnostat™ Sensor
4989	Airway Adaptor
8751	Sensor Cable Holding Clips

2.0 Maintenance Schedule

2.1 General

All Novametrix Medical Systems Inc. equipment is warrantied for a period of one year from the date of shipment. However, to insure the functional integrity of the monitor, Novametrix recommends the following maintenance schedules be adopted with regard to the Model 7000.

At the customers request, Novametrix will provide repair and calibration services under the terms of a Service Contract. Contact the Novametrix Service Department at 1-800-243-3444 (in Connecticut call Collect 203-265-7701) for contract details.

2.2 Battery Maintenance

The monitor was shipped from the factory with a fully charged battery. Since the monitor draws some battery power even while turned off, it is recommended that the monitor be operated on line power for the first 24 hours to allow ample time for the battery to fully recharge.

In the case of prolonged periods of storage or shipment the battery may discharge to a point where the unit will not turn on. Should this occur, plug in the line cord, set the switch on the rear panel to the | position, turn the monitor off (ensure that the green "AC" LED on the front panel is illuminated), and allow the monitor to charge for 24 hours before switching it on.

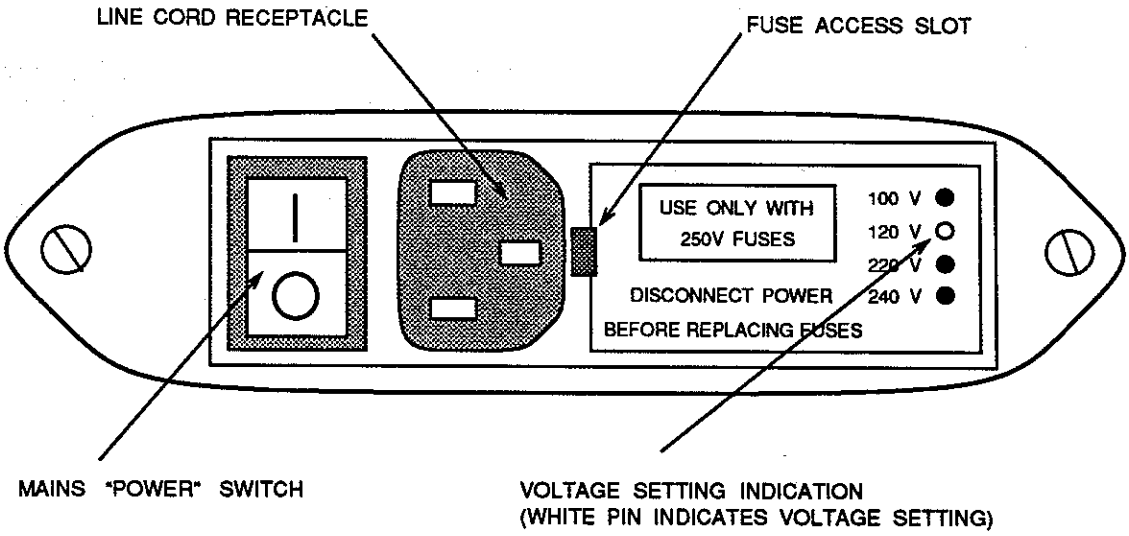
To insure maximum battery life and performance, the Model 7000 should be operated in the battery mode (line cord disconnected) at least once each month. The unit should be operated in this mode until the "Low Battery" indicator appears on the CRT screen. The line cord should then be reconnected and the battery given sufficient time to recharge. The monitor may be operated normally on line power while the battery is recharging. Approximately 24 hours are required to fully recharge a discharged battery.

Every six months the battery should be visually inspected for defects including but not limited to, swollen or misshapen sides, leaking battery acid, exposed conductors or frayed insulation. If any of these conditions exist, contact the Novametrix Service Department for a battery replacement. Replacement batteries are subject to a replacement charge.

2.3 Fuses and Line Cord

Should the fuse(s) need replacement be sure to replace with the same type and rating; 250 V 2A slow-blow for 100V and 120V units; 250 V 1A slow-blow for 220 V and 240 V units. The fuse is accessed from the power entry module located on the rear panel, ensure

the mains switch is in the **O** (off) position when replacing the fuse. Place a small screwdriver into the FUSE ACCESS SLOT and pry the fuse block off to expose the fuse(s).



The line cord supplied is a tested "HOSPITAL GRADE" type, avoid using other types of cords, if the cord is damaged or frayed contact Novametrix Service Dept. for a replacement. Ensure the unit is plugged into a grounded hospital-grade outlet, under no circumstances should the ground pin on the plug be bypassed.

2.4 Cleaning the Model 7000

To clean the Model 7000, turn off system power and unplug the line cord. Dampen a cloth with isopropyl alcohol and wipe the dirty areas of the unit until cleaned. Dry with a clean cloth or a paper towel.

Caution: do not submerse the unit or sensors in liquid to clean!

The same applies for the Capnostat™ CO_2 and SaO_2 Saturation sensors. It is imperative that the sapphire windows on both the Capnostat™ sensor and the airway adaptor be free from any residue including moisture, for proper operation. Before calibrating the sensor check the ZERO and SPAN cells for contamination, also check the sensor's windows for dirt.

3.0 Operational Tests

3.1 Overview

Operational testing for the Model 7000 should be performed on each monitor before it is placed into the clinical environment. The tests may also be used to spot check the unit in the event a malfunction is reported. This test verifies the overall operation of the monitor and sensors (this test does not verify performance accuracy of the monitor, see Calibration and Adjustments for such tests). Should the unit fail any of these tests contact the Novametrix Service Department.

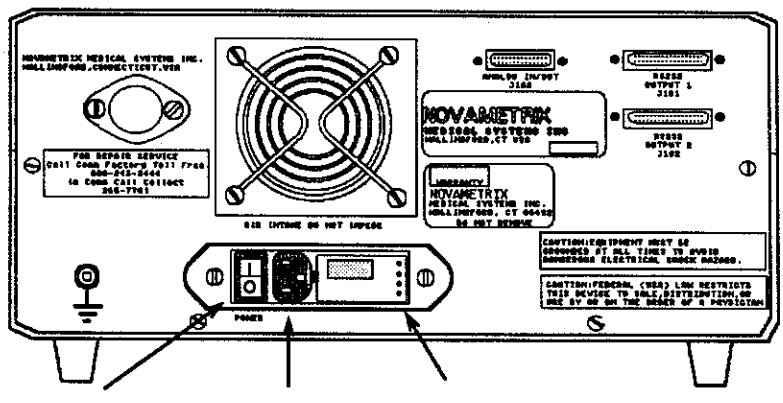
3.2 Equipment Required

- Line cord (supplied with unit) PN 600026
- Capnostat™ Sensor with Airway Adaptor
- SaO_2 Sensor (SuperBright™)
- AC Current leakage tester*
- Hipot Tester*
  * Calibrated and N.B.S. traceable

3.3 Monitor Tests

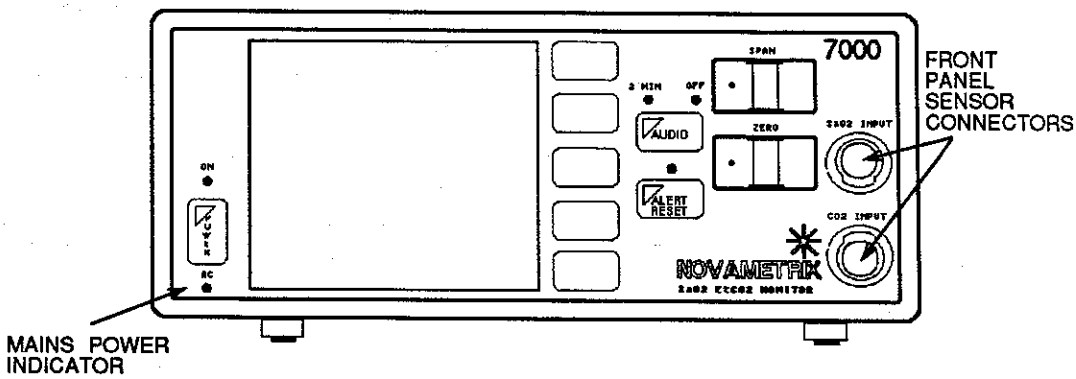
NOTE: The following steps will enable the technician to verify the operation of the sensors and will describe the various options and menus that are part of the system operation. The items in **BOLD FACE** indicate the button to be pressed that flow with the procedure, at times optional buttons are listed and explained in parenthesis which are alternative selections (but will remove the technician from the flow of the procedure). For a more in-depth explanation of the operation and screen formats of the unit please refer to the Operating Manual.

3.3.1 Inspect the unit for any damage, shake it and verify there is no loose hardware inside. Check that the rear panel power entry module is set for the proper voltage, set the mains switch to the **O** position.



3.3.2 Inspect the line cord, verify no frayed wires or other damage, plug the line cord into the rear panel power entry module.

3.3.3 Verify that the Capnostat™ and SaO_2 sensors are undamaged, plug each sensor into the appropriate front panel connector.



3.3.4 Place the mains power switch to the I position. Verify the green "AC" LED on the front panel illuminates.

3.3.5 Apply power to the unit by pressing the **POWER** button on the front panel. Verify the green "ON" LED on the front panel illuminates. Verify the "Sensor warm up" window appears and then disappears when the proper temperature is reached and the temperature stabilizes (temperature is indicated by black coloration of the vertical bar in the window).

3.3.6 Press and hold the **AUDIO** button on the front panel for approximately five seconds until the yellow "OFF" LED above the button illuminates.

3.3.7 Press and hold the **Run/Freeze** softkey until "MONITOR PARAMETERS" menu appears. Select **Calibration Settings**, using the **CAL MODE** softkey highlight "Cal with cal cell". Press **Exit**.

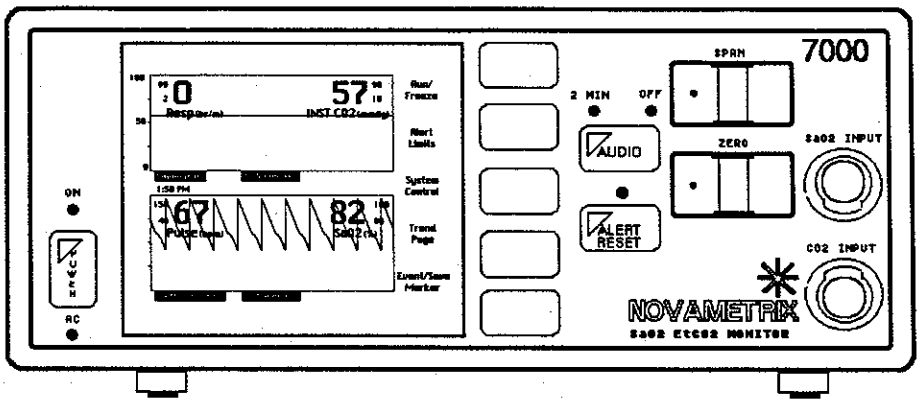
3.3.8 Place the Capnostat™ sensor into the zero cell and verify that "Sensor ZERO in Progress" is displayed with a minute:second counter that counts down.

3.3.9 Once the zero is complete "Sensor ZERO Complete Place sensor in SPAN cell" will be displayed on the screen. Remove the Capnostat™ sensor from the ZERO cell and place it in the SPAN cell. Verify that "Sensor SPAN in Progress" is displayed.

3.3.10 When the span is complete the following message will be displayed; "Sensor SPAN Complete Please remove the sensor from the cell" remove the sensor and verify all the message windows disappear. Place the sensor back into the SPAN cell and check that a waveform moves from right to left with an "INST CO2 (mmHg)" value equal to the Span Cell value (this assumes that the unit is

not set up for digital display). Press **Cancel Airway Zero** to remove the airway zero menu.

3.3.11 Place the SaO_2 sensor on your person in accordance to the type that is used. Consult the instructions supplied with the sensor for proper application. Verify that after a few seconds the Plethysmogram waveform appears with values for both "Pulse" and "SaO2 (%)". A tone will sound with each pulse waveform peak (unless the Audio Pulse has been defeated from the "AUDIO PULSE MENU"). If any of the values are outside of the current limit setting the "ALERT RESET" LED will flash (no audio will sound because it was defeated in step 3.4.2).
The screen should resemble the diagram below, the actual values will vary but the waveform appearances should be similar.



3.3.12 Press the **Run/Freeze** softkey, verify that the waveform freezes and "WAVEFORMS FROZEN" appears at the upper left of the screen. Remove the SaO_2 sensor from your finger, "Probe Off Patient" and "ALERT" will appear in the Plethysmogram waveform window, the "ALERT RESET" LED will flash, and the "Pulse" and "SaO2" values will be 0.

3.3.13 Press the **AUDIO** button, verify an alert sounds. Press **ALERT RESET** and verify the sound stops and the "ALERT RESET" LED goes off. Press and hold **AUDIO** until the yellow "OFF" LED illuminates.

3.3.14 Press the **Exit** softkey, verify that the waveforms are no longer frozen.
Press **Alert Limits**, check that an ALERT MENU appears.
Select **CO2 Alert Limits** and verify the CO2 ALERT LIMITS window appears. The limits can be changed by using the **Move Selection Bar** to highlight the desired parameter and **Increase**, **Decrease** to vary the value of the parameters:

RR High Limit = 5 to 200
RR Low Limit = 0 to 100
CO_2 High Limit = 5 to 100
CO_2 Low Limit = 0 to 95

Set the CO_2 parameters to the desired values then press **Previous Menu** (the **Exit** softkey will return the user to the real-time display).

3.3.15 Select **SaO2 Alert Limits** and verify that a "SaO2 ALERT LIMITS" menu appears. The limits can be changed by using the **Move Selection Bar**, **Increase**, and **Decrease** softkeys:

Pulse High Limit = 35 to 250
Pulse Low Limit = 30 to 245
SaO2 High Limit = 20 to 100
SaO2 Low Limit = 0 to 95

Set the SaO2 parameters to the desired values then select **Previous Menu**. When the "ALERT MENU" is shown press **Exit**.

3.3.16 Select the **System Control** softkey. Verify that the "CONTROL MENU" window appears then select **SaO2 Controls**. Verify the "SaO2 MENU" appears, select **Audio Pulse**. When the "AUDIO PULSE MENU" appears the **AUDIO PULSE** level bar will appear. The status of the monitor will be that of the level highlighted even after power is removed, unless the monitor is powered up in default mode or it is deliberately changed. Press the **Previous Menu** to return to the "SaO2 MENU" (or **Exit** to return to the real-time waveforms).

3.3.17 At the "SaO2 MENU" select **Configure Display**, the "CONFIGURE SaO2 DISPLAY" window enables the following parameters to be changed simply by pressing the associated softkey. By pressing **Averaging** a "SaO2 / PULSE AVERAGING" options window will appear where both SaO2 averaging and pulse averaging times can be selected, press **Previous Menu** (exiting to real-time display can be done through **Exit**). The **Update Timer** acts as a toggle switch to activate or deactivate this function. The **Speed** softkey will control the scrolling speed of the waveform in the Plethysmogram waveform window only. To exit this window press **Previous Menu** to return to the "SaO2 MENU" then press **Previous Menu** once again to get to the "CONTROL MENU" (press **Exit** to return to viewing real-time waveforms).

3.3.18 From the "CONTROL MENU" select **CO2 Controls** to bring up the "CO2 MENU". From this menu the user can select **Compensate** which will bring up the "COMPENSATION" window for corrections of N20 Compensation and O2 Compensation along with the **Barometric Pressure** softkey which brings up the "BAROMETRIC PRESSURE" window. The barometric pressure's setting is changed by pressing the **Increase** or **Decrease** softkeys, these will either increment or decrement the value in steps of 10 within the limits of 560 - 760mmHg. (To leave the user can select **Previous Menu** to return to the "COMPENSATION MENU" or **Exit** to view real-time waveforms). Press the **Previous Menu** softkey to return to the "COMPENSATION MENU" then press it once again to return to the "CO2 MENU".

3.3.19 The **Configure Display** softkey will bring up the "CONFIGURE CO2 DISPLAY MENU". Here the **Averaging** softkey will bring up the "AVERAGING" menu. This enables the user to select "End Tidal Averaging" from one of four options (Instantaneous, Breath to Breath, 2 Breath, 4 Breath) by repeatedly pressing the **End Tidal** softkey. The "Resp. Rate Averaging" can be set to one of three

options (Breath to Breath, 2 Breath, 4 Breath) by pressing **Resp Rate**. Press the **Previous Menu** softkey to return to "CONFIGURE CO2 DISPLAY".

3.3.20 The **Scale** softkey will toggle the scale from one of two options (0-50, 0-100). The **Speed** softkey will select one of three speeds that will affect only the Capnogram real-time waveform (amplitude vs. time). Press **Previous Waveform** to return to "CO2 MENU", press **Previous Menu** again to reveal the "CONTROL MENU".

3.3.21 Selection of the **Setup** softkey will present the "SETUP MENU", here the user can choose to enter the "AUDIO FEATURES" or "INTERFACES" option windows by pressing the appropriate softkeys. Press the **Audio Features** softkey and the "AUDIO FEATURES" window will appear with the options to select one of three levels for "Alert Volume" (by pressing the **Audio Features** key), and the option of having the "Keyclick" on or off (toggle function). Press **Previous Menu** to return to the "SETUP MENU".

3.3.22 The **Display Controls** softkey from the "CONTROL MENU" will bring up the "DISPLAY CONTROLS" window. By pressing the **Display View** softkey the screen representation of the real-time waveforms will be changed to either an analog amplitude vs. time (waveform), a triple waveform, or a bargraph display(digital). (NOTE: the "Run / Freeze" is not an option in the digital mode). Either of the three choices will remain in memory and be stored even if the unit is turned off, however the default is the waveform option (amplitude vs. time). Press the **Previous Menu** to return to the "SET UP" menu.

3.3.23 Press the **Interfaces** softkey to reveal the "INTERFACES" window. This window enables the user to control the status of the three connectors located on the monitor's rear panel. Either of the two RS232 ports can be programmed for Dinamap, or HP Think jet Printer, or Capno to Mac by pressing the appropriate softkey (toggle function).
The sampling system option can also be activated here if it is installed. If the **Sampling System** softkey is depressed and the option is not installed then "Pump Inoperative" will be displayed.
The **Analog Output** softkey will display the "ANALOG OUTPUT" menu when pressed. Pressing **Select Channels** enables each of the three output channels to be assigned to one of six parameters. The **Move Selection Bar** will highlight the desired parameters consecutively with each depression. The **Toggle Channel** will:

- turn the highlighted parameter off if it is assigned a channel,
- assign the parameter a channel if it was off and there is an available channel (only three channels are available, it will assign the lowest number first),
- will toggle the number of the assigned channel if more than one channel is available,
- will not assign any channels to the parameter if all three channels are already assigned.

(The **Clear All Channels** will turn all parameters off even the highlighted parameter for reassignment of channel numbers. All the options chosen will be saved in memory and will remain in memory unless deliberately changed, or if the monitor is powered up in default mode.)

3.3.24 Press **Previous Menu** to return to "ANALOG OUTPUT". Select **Calibrate Channels** to bring up the "ANALOG CALIBRATION MENU" window. The actual channel numbers and the assigned parameters will be displayed, there will also be a "VALUE" column. The value column will show one of three values depending on the parameter chosen and the "Scale" setting (highlighted). Press the **Toggle Scale** and the Scale will change from ZERO to HALF to FULL with each depression. The corresponding pin on the rear panel connector will output the corresponding voltage that represents either ZERO, HALF, or FULL scale. Press **Exit** to return to the real-time display.

3.3.25 The **Trend Page** softkey changes the entire screen display to show four trend waveforms (Resp. Rate, Pulse, End Tidal, SaO2). From this display **Trend Parameters** will bring up a window that enables the "DURATION" and "SCALE" of the trend to be changed by pressing the appropriate softkey press the **Exit** softkey to return to the "Trend Page".

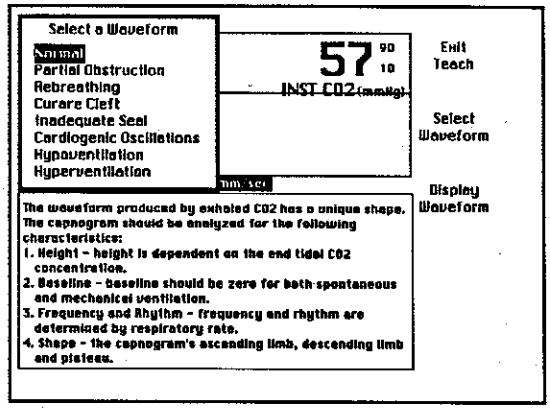
3.3.26 Pressing **Trend Expansion** will enable selection of one of the four trend waveforms to be selected by pressing **Next Trend.** Once the desired waveform has been chosen it can be expanded by pressing **Expand Trend.** The display will change to show the chosen waveform and a 12 minute expansion. The **Left** and **Right** softkeys will control the cursor movement. **Print Screen** will reproduce the current screen display provided the HP Think jet printer is connected and the RS232 output has been programmed properly. Press the **Previous Menu** to return to the four waveform display.

3.3.27 The **Clear Trend** softkey will clear all trend information in all four windows, because of this a prompt window will appear to verify that the trend information is to be erased, press **No** to return to the "Trend Page" (**Yes** will erase all Trend Information).

3.3.28 Press **Exit Trend** to return to the real time display. Press the **Run/Freeze** softkey, verify the waveforms freeze.

3.3.29 The **Compare Waveform** softkey will enable the user to compare a stored waveform with the current waveform, provided that the **Event/Save Marker** softkey was pressed to save an earlier waveform. If no data was saved then "No Compare Data Saved" will appear in the "Saved Capnogram" window. The **UnFreeze Waveform** softkey will allow real time viewing of the Capnogram waveform. Press **Freeze Waveform** to toggle back to a frozen display.

3.3.30 Press **Exit Compare Waveform** to exit, select **Teach Mode** (waveforms must be frozen). The following screen will appear:


Select a Waveform
Normal
Partial Obstruction
Rebreathing
Curare Cleft
Inadequate Seal
Cardiogenic Oscillations
Hypoventilation
Hyperventilation
57
90
10
INST CO2(mmHg)
Exit Teach
Select Waveform
Display Waveform
The waveform produced by exhaled CO2 has a unique shape. The capnogram should be analyzed for the following characteristics:
1. Height - height is dependent on the end tidal CO2 concentration.
2. Baseline - baseline should be zero for both spontaneous and mechanical ventilation.
3. Frequency and Rhythm - frequency and rhythm are determined by respiratory rate.
4. Shape - the capnogram's ascending limb, descending limb and plateau.

The **Exit Teach** will bring the user back to the previous display.
The **Select Waveform** will toggle between each of the eight choices. Once a selection has been made, **Display Waveform** will display an example of the selection.

3.3.31 Once the selected waveform is displayed, the following options are available;
Text: will display a description of the chosen waveform.
Next Waveform: will toggle to the next choice.
Print Screen: will print the screen display provided the HP Think jet is properly connected.
Teach Mode: will display the previous screen display.

3.3.32 Press the **Exit** softkey to return to the "WAVEFORMS FROZEN" display.
Press **Exit** again to return to real time display.

3.3.33 The **Event/Save Marker** softkey will place a pointer arrow on both real-time waveforms when pressed. The pointer arrow will not be visible on the digital display when pressed. These pointers are stored with the waveforms in trend memory and can be seen on the trend waveforms when in Trend Mode.
The waveform will also be stored for comparison in the "Compare Waveform" mode.

3.3.34 Remove the Capnostat™ sensor from the Span Cell and attach the airway adaptor to the sensor. Slowly breath through the airway adaptor so as to produce a waveform on the screen.
Check the waveform for erratic noise and dropouts.
Verify steady response and a "Resp(br/m)" value other than zero.

3.3.35 Check the "Resp(br/m)" and "ETCO2" (the "INST" option may be enabled here instead) values to see if they are within the limits presently listed, if they are press **AUDIO** and verify the yellow "OFF" LED goes out.. If not, edit the limits so as to avoid setting an alarm due to "Resp(br/m)" or "ETCO2" values out of range.

- Press **Alert Limits**, then press **CO2 Alert Limits**. At the "CO2 ALERT LIMITS" window use the **Move Selection Bar, Increase,** and **Decrease** softkeys to edit the limits to the required values. Return to the Real time display by pressing **Exit**. Begin breathing into the airway adaptor as before until a "Resp" value is present.

3.3.36 Stop breathing into the airway adaptor.

3.3.37 Verify that after a while "ALERT" is displayed on the screen and a continuous tone sounds from the unit.
Verify the "Resp(br/m" value is zero.
Check the upper right portion of the screen for "No Respiration" followed by a minute:second counter which will increment.

3.3.38 Verify the "ALERT RESET" LED on the front panel blinks.

3.3.39 Press the **AUDIO** button on the front panel.
Confirm that the continuous tone stops.
Verify that the 2 MIN LED illuminates.

3.3.40 Press the **AUDIO** button again.
Verify the continuous tone returns.

3.3.41 Press and hold the **AUDIO** button for five seconds, verify that the yellow "OFF" LED illuminates and the tone stops.

3.4 Safety Checks

3.4.1 Power down the monitor by pressing the **POWER** button on the front panel. Place the mains power switch on the rear panel to the **O** position and unplug the line cord from the wall socket.

3.4.2 Place the mains switch located on the rear panel to the | position.
Measure the leakage current from the monitor's chassis with the unit on and the line cord:

- grounded,
- ungrounded,
- ungrounded and polarity reversed.

3.4.3 Verify the leakage does not exceed 25 µA (50 µA for units operating at 220 / 240 VAC).

3.4.4 Apply 2.5 KV between the Hot and Neutral sides of the line cord (shorted together) and chassis ground for no less than 1 minute. Verify no arcs or leakage.

3.4.5 Apply 1.5 KV between the chassis ground and the pins on the "SaO2 INPUT" connector (shorted together) for no less than 1 minute. Verify no arcs or leakage.

4.0 Calibration and Adjustments

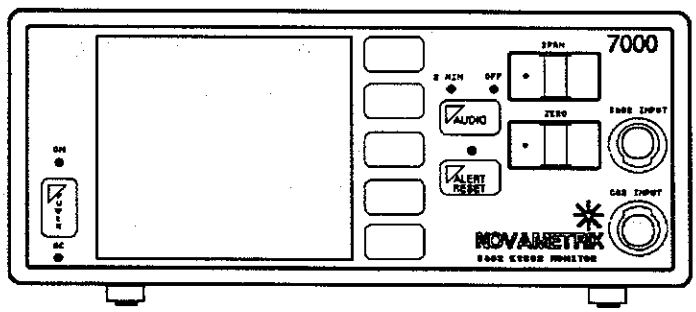
4.1 Introduction

The Model 7000 is a highly complex microprocessor controlled monitoring unit. The internal electronics of the unit require no regular scheduled maintenance or calibration (except battery and fuses), all required adjustments are performed at the factory by Novametrix trained technicians. In order to verify the accuracy of the monitor the following Calibration procedure was included which would determine any possible malfunctions with the unit. Should any problems occur the Adjustment procedure will aid in isolating the problem. The adjustment tests should only be performed by qualified service personnel, or returned to the Novametrix factory for repair. Please contact Novametrix Service Dept. before returning any equipment to the factory.

In order to correctly calibrate the Model 7000 SaO_2 section the TB500A test box is required. The TB500A simulates various saturation levels at different signal strengths along with faulty probe conditions. The TB500A is the only acceptable method of verifying the accuracy of the SaO_2 section and is available from Novametrix Service Department.

4.2 Calibration Procedure

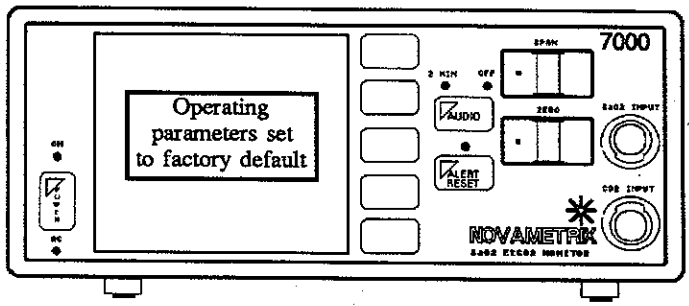
Before proceeding with the Calibration Procedure it is suggested that the currently stored parameters be recorded so that the monitor can be returned in the manner with which it was received. If the monitor has not been used (just received from the factory) then the parameters will be at the default settings. To record the current parameter settings perform the following;



- Apply power (see steps 4.2.2-4.2.4 of this section). Press the **Run** softkey. Press and hold the **Run/Freeze** softkey until the "MONITOR PARAMETERS" window appears. Record the parameters.

The following procedure assumes the unit is set to its default settings, these are listed below. The monitor can easily be reset to these settings by simultaneously pressing

the **ALERT RESET** and **POWER** buttons located on the front panel until the following screen appears.



Note: The span cell value will default to 57 mmHg. However, this setting will be adjusted to the particular span cell value, as listed on the front of the span cell or on the rear of the monitor, before the monitor is shipped. *It is important that the correct value be entered if the unit is to operate correctly*.

Default Settings

Alert Limits: $ETCO_2$ 90-10, Resp 99-2, SaO_2 100-80, Pulse 150-40

Audio Features: Alert Volume-High, Keyclick-On

Audio Pulse Beep (SaO_2 portion): High

CO_2 Calibration: Cal with cal cell (not with gas), span cell value set to 57 mmHg

Note: The span cell value will default to 57 mmHg. However, this setting will be adjusted to the particular span cell value, as listed on the front of the span cell or on the rear of the monitor, before the monitor is shipped. It is important that the correct value be entered if the unit is to operate correctly.

Compensation (CO_2 portion) : O_2 < 60%, N_2O-No, Barometric Pressure-760 mmHg

Display Screen: Waveform view, CO_2 scale 0-100 mmHg, display speed 12.5 mm/sec

Display Parameter (CO_2): $ETCO_2$ displayed (not INST CO_2)

Display Averaging: End Tidal and Resp. Rate-4 Breath Averaging, Saturation and Pulse Rate-8 second averaging.

No-Saturation-Update Timer: on

Trend Page: Duration-4 hours, display scale-full ($ETCO_2$ 0-100, Resp 0-150, SaO_2 50-100, Pulse 0-250)

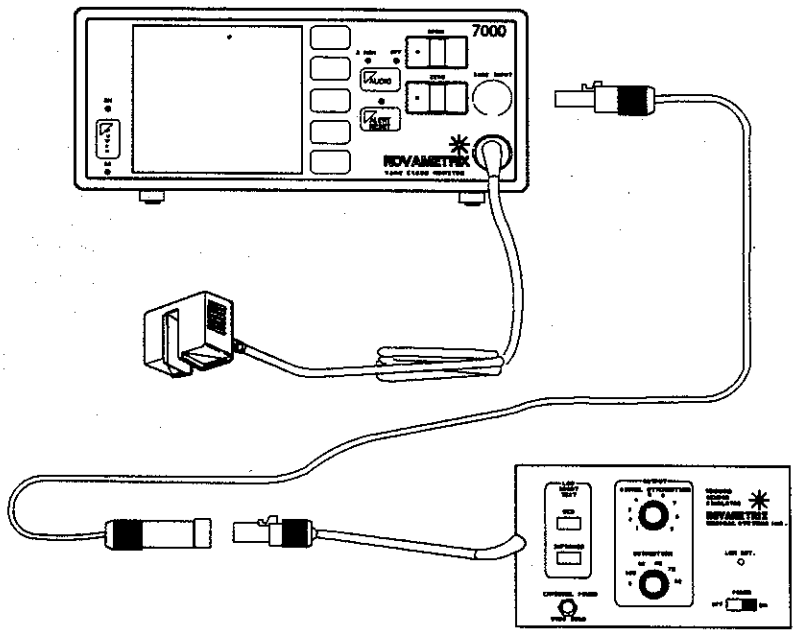
4.2.1 Equipment required

- AC Power Cord (supplied with unit). PN 600026
- Capnostat™ Sensor with 3 Airway Adaptors.
- TB500A Sensor Simulator with SuperBright™ adaptor cable.*
- Hipot Tester **
- Leakage Meter **
- D.V.M.**
- Oscilloscope**
- Gas Calibrator with 5% & 10% CO_2 *

*Available from Novametrix Service Dept.
** Calibrated and N.B.S. traceable.

4.2.2 Attach the line cord to the unit, set the mains switch on the rear panel to the | position. Verify the green "AC" LED on the front panel illuminates.

4.2.3 Plug the Capnostat™ Sensor into the "CO_2 INPUT" jack on the front panel. Plug the TB500A into the "SaO_2 INPUT" jack on the front panel.



4.2.4 Turn the monitor on by pressing the **POWER** button on the front panel. Verify the green "ON" LED on the front panel illuminates. When the screen comes up check for "Capnogram", "Plethysmogram", and "Sensor warm up" waveform windows. With the main menu displayed press the **Run** softkey, then press and hold the **Run/Freeze** softkey until "MONITOR PARAMETERS" appears. Select **Calibration Settings**, then press **CAL MODE** until "Cal with cal cell" is highlighted. Press **Exit** to return to the main menu.

4.2.5 Once the sensor is up to temperature, place the Capnostat™ Sensor into the ZERO cell and wait for "Sensor ZERO Complete Place sensor in SPAN cell". Place the sensor into the SPAN cell, when "Sensor SPAN complete Please remove the sensor from the cell" appears remove the sensor, as soon as the instruction windows disappear place the sensor back into the SPAN cell.
Press **Cancel Airway Zero.**
Verify a waveform moves from right to left and that the "INST CO2(mmHg)" value is equal to that of the SPAN Cell value. Ensure the waveform is steady with no spikes or dropouts.

4.2.6 Set the unit to display Instantaneous CO_2 as follows:

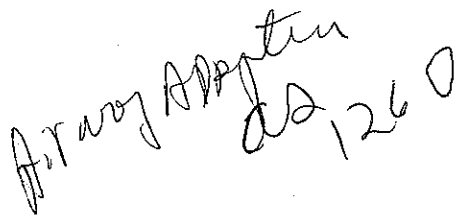
- From the main menu press **System Control**, press **CO2 Controls** at the "CO2 Menu" press **Configure Display**, then select **Averaging**, use **End Tidal** to highlight "Instantaneous (INST CO2)". Press **Exit.**

4.2.7 Press and hold **Run/Freeze** until the "MONITOR PARAMETERS" window appears (the CPU software revision level can be read from here).

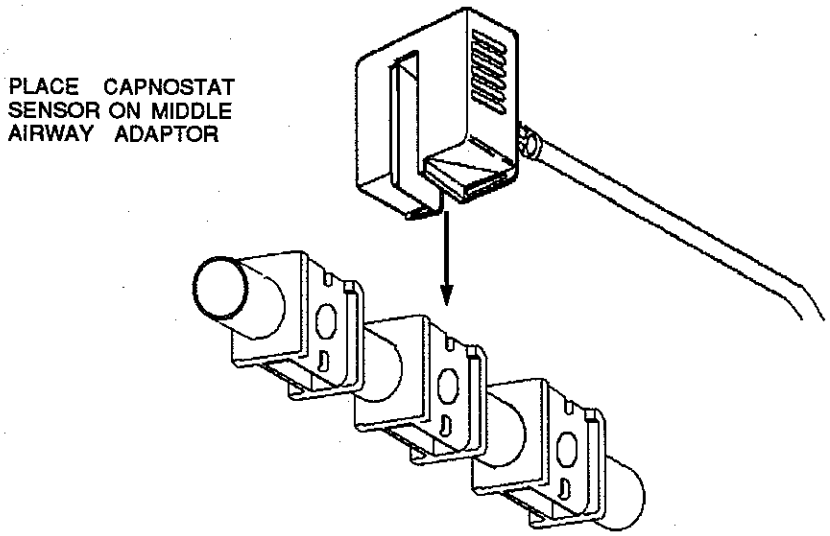
4.2.8 Press **Display Parameter**, the "SENSOR STATUS" will appear and a "no error" message should be displayed. Verify the other parameters are set as required (refer to Error Messages section). Press the **Previous Menu** softkey to return to "MONITOR PARAMETERS".

4.2.9 Press the **Calibration Settings** softkey to bring up the "CALIBRATION SETTINGS" window.
Press **CAL MODE** so as to highlight "Cal with gas", press **CAL GAS** until "5% CO2" is highlighted, then press **Exit.**
When the main screen appears press **System Control**, then select **CO2 Controls.**

4.2.10 At the "CO2 MENU" select **Calibration**, remove the sensor from the SPAN cell and attach it to the airway adaptor. Set the sensor in a place where it will not be introduced to any CO_2 gas.
Press **Zero**, wait for the Zero process to end, then attach the gas calibrator to the airway adaptor and set it for 5% CO_2. Let the gas flow for a few minutes



then press **Span.**



When "Calibration Complete Press RUN to Continue" appears press **Run.** Verify a steady waveform as before with a CO_2 value between 36 - 40.

4.2.11 Apply 10% CO_2 gas through the sensor/airway adaptors, verify the waveform gradually rises to a value of 72-79 (Resp should remain at 0).

4.2.12 Set the TB500A SATURATION to **92**, and the SIGNAL ATTENUATION to **3**. Switch the TB500A power switch **ON**.
Verify that a pulse value of 60 ± 1 and an SaO_2 value of 92 ± 2 are displayed. A Plethysmogram waveform should be present with a tone sounding for each waveform peak (provided the SaO_2 audio pulse has not been defeated).

4.2.13 Press the **AUDIO** button and hold it until the yellow "OFF" LED above the button illuminates (to avoid alarm sounding during the next test).
Vary the controls on the TB500A as listed in the table and verify the monitor's responses and tolerances

ATTENUATION	SATURATION	SaO_2 VALUE	SuperBright™ Sensors
9	100	98-100	98-100
9	92	88-96	88-96
9	82	78-86	80-88
9	72	68-76	74-80
9	62	not specified	not specified
3	100	99-100	99-100
3	92	90-94	90-94
3	82	80-84	82-86
3	72	70-74	75-79
3	62	60-64	67-71

NOTE: SuperBright sensors will read differently with the TB500A test box, follow the "SuperBright Sensors" values for SuperBright Model 7000, use the "SaO_2 VALUE" values for non-SuperBright Model 7000.

4.2.14 Return the ATTENUATION to **3** and the SATURATION to **92** on the TB500A. Press **ALERT RESET** to cancel the alert status.

4.2.15 Press **System Controls**, when the "CONTROL MENU" appears press **Setup** to bring the "SETUP MENU". Select **Interfaces** then select **Analog Output** at the "INTERFACES" window.
Press the **Select Channels** softkey, when "SELECT ANALOG CHANNELS" appears verify that Capnogram is assigned Ch1; End Tidal is assigned CH3; and Resp. Rate is assigned CH2 (these are the default settings).

4.2.16 Press **Previous Menu** to return to the "INTERFACES" window. Select **Calibrate Channels**, verify that a "ANALOG CALIBRATION MENU" appears.
Measure the outputs on J103 (rear panel connector), with the "Scale" set to ZERO (Scale is changed by pressing **Toggle Scale**), verify the outputs (pins 2 for CH1; 10 for CH2; and 9 for CH3) are all zero volts.

4.2.17 Verify proper HALF and FULL scale voltages at the output by pressing **Toggle Scale** to switch from ZERO to HALF to FULL. The values are listed below:

PIN (Channel)	PARAMETER	HALF/FULL VALUES
2 (CH1)	Capnogram	1.96 volts/3.92 volts
10 (CH2)	Resp. Rate	1.96 volts/3.92 volts
9 (CH3)	End Tidal	0.98 volts/1.96 volts

4.2.18 Press **Previous Menu** .to return to "ANALOG OUTPUT", then select **Select Channels.**
Press **Clear All Channels**, verify that all the parameters are "OFF". Use the **Move Selection Bar** to highlight Plethysmogram, then press **Toggle Channel** to assign it CH1.
Use the **Move Selection Bar** to highlight Saturation, press **Toggle Channel** to assign CH2.
Press **Move Selection Bar** to highlight Pulse Rate, Assign CH3 by pressing **Toggle Channel.**

4.2.19 To return to the "INTERFACES" menu press **Previous Menu**, select the **Calibrate Channels** softkey, verify the parameters are assigned as described earlier.

4.2.20 Confirm the proper ZERO, HALF, and FULL voltages by pressing the **Toggle Scale** softkey to change the Scale.

PIN (Channel)	PARAMETER	HALF/FULL VALUES
2 (CH1)	Plethysmogram	1.24 volts/2.49 volts
10 (CH2)	Saturation	0.98 volts/1.96 volts
9 (CH3)	Pulse Rate	2.48 volts/4.96 volts

4.2.21 Press the **Exit** softkey to return to the real-time display. Power down the unit by pressing the **POWER** button on the front panel.

4.3 Adjustment Procedure

The following procedure should only be performed by qualified personnel in the event a malfunction or breakdown occurs with the unit. The electronics used in the Model 7000 are highly sensitive to static electricity and proper grounding techniques should be adhered to at all times when handling the internal components. Please consult the following section "Assembly and Disassembly Instructions" when performing repairs or adjustments on the monitor. In addition to the steps and tests listed here the "Theory of Operation" section holds several bits of necessary information and possible test points to check on suspect boards.

4.3.1 Equipment Required:

- Line cord (supplied with unit) PN600026
- TB500A Sensor Simulator with SuperBright™ adaptor cable.*
- 2410-01 (digital bds.); 2411-01 (input bds.) extender cards.*
- Oscilloscope**
- D.V.M.**
- Capnostat™ Sensor

* Available from Novametrix Service Dept.
** Calibrated and N.B.S. traceable.

4.3.2 Follow the disassembly instructions in the following section (ensure the line cord is disconnected and no power is applied to the unit), remove all the boards from the card cage and set aside (ensure proper static control handling). Boards to be removed from the card cage:

- Memory
- CPU
- Video
- CO_2 Front End (two board combo)
- SaO_2 Front End (two board combo)

4.3.3 Remove the Power Supply board and disconnect the battery. Attach the line cord to the rear panel and place the mains switch in the | position ("AC" LED on the front panel will not light). Using the D.V.M. measure the voltage between "GND" and "REG OUT" test points on the Motherboard found to the right of the CRT. Verify +14.5 volts ± .002 volts, adjust VR1 on the Motherboard if necessary. Set the mains switch on the rear panel to **O**.

4.3.4 Install the Power Supply board, set the mains switch on the rear panel to |. Verify the "AC" LED illuminates. Press the **POWER** button on the front panel, verify the "ON" LED illuminates, the CRT lights up (retrace lines will be visible with no video), and the fan turns on. Monitor the following test points on the power supply board, use the GND point on the board as ground reference.

-15 V TP..... -14.5 V to -15.5 V
+15 V TP..... +14.5 V to +15.5 V
+5 V TP..... +4.9 V to + 5.1 V
RDC TP..... +18 V to +25 V
PCV TP..... +13 V to +15V

NOTE: Both VR1 (low BAT turn off point) and the "VOLTAGE ADJUST" points on the board are factory set to special tolerances and should not require further adjusting.

4.3.5 Press the **POWER** button on the front panel, verify the unit powers down. Replace the CPU, Memory, CO_2 Front End, and SaO_2 Front End boards into their appropriate card slots. Press the **POWER** button and verify the screen appears. The screen will appear "wavy" unless the battery is connected and in working order, therefore reconnect the battery.

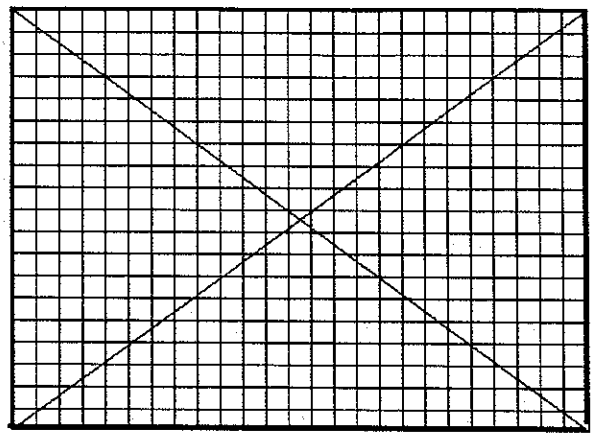
4.3.6 If the screen is not stable then the CRT requires alignment, this is done in the following manner:

- Power down the monitor.
- Install the card extender in the Video Board's slot then attach the Video board to the card extender.
- Install a SPDT switch in line with pin A21 on connector P206 (to switch the line either in or out of circuit).
- Toggle the SPDT switch so the line is out of circuit (open), then apply power to the monitor.
- Adjust the H HOLD potentiometer on the CRT board so that the video display is vertical and stationary or slowly rolling.
- Toggle the SPDT switch so the line is in circuit (closed), verify the video is locked on screen.
- Seal the adjustment on the CRT board.

4.3.7 The remaining controls on the CRT are factory adjusted and should require no further tuning (consult "Theory of Operation" for more information). For proper geometric alignment of the CRT, a test grid is stored in video memory which will help in adjusting the yoke's magnets to acquire the best possible screen. To access this screen perform the following:

- Press **Run** from the waveform screen.
- Press and hold the **Run/Freeze** key to freeze the waveforms, a "MONITOR PARAMETERS" window will appear.
- Select **Display Parameters**, when the "SENSOR STATUS" window appears press the third softkey from the top (it will not be labelled),

the following diagram will appear on the screen:



To exit press any of the softkeys and the "SENSOR STATUS" window will reappear. Press **Previous Menu** to return to the "MONITOR PARAMETERS" window (or press **Run** to return to the waveform displays).

4.3.8 Press the **Time Date** softkey if requires adjustment, the **Select Parameter** will highlight the parameter to be changed and editing is done through the **Increase** and **Decrease** keys. Press **Run** to return to the waveform display.

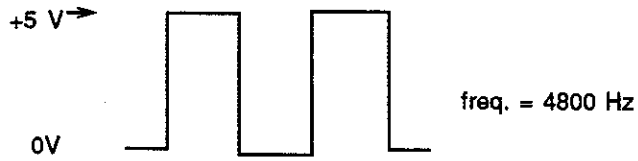
4.3.9 Power down the unit and place the CO_2 Front End boards on a card extender. Then power the unit back up. Check the LED on the 2421 board (larger) and verify that it blinks on and off at approximately 1 Hz (if it stays continually on or flashes at a much faster rate there is most probably a problem with the microprocessor circuitry on board, try turning the power off then on again).

4.3.10 Monitor TP4 (TEMP) on the 2418 CO_2 Front End board, use TP2 (GND) as ground reference. Plug the Capnostat™ sensor into its appropriate jack on the front panel. The voltage should start at ≈ -5 volts and then rise to approximately +5 volts, then it will stabilize ≈3.5 volts.

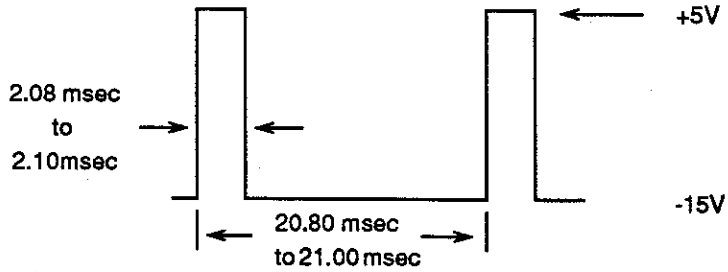
4.3.11 Measure the following points on the 2418 board (smaller of the two CO_2 Front End boards) with the D.V.M.

P3-19	-15 volts
P2-22	+15 volts
P3-25	+5 volts
TP10 (HTR)	3.5 volts
TP5 (-80 VOLTS)	-80 volts ± 3 volts (only when sensor is installed)

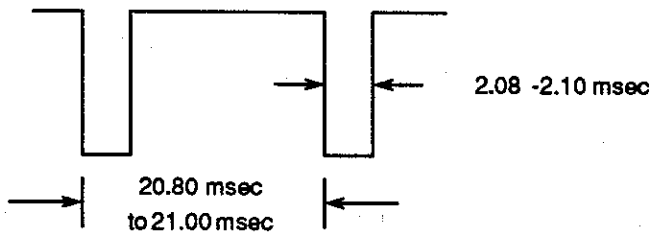
4.3.12 Monitor P3-14 with the oscilloscope, verify the following waveform:



4.3.13 Monitor TP11 (VS) on the board under test, verify the following waveform:
NOTE: If the pulse width is out of specification check tolerance of C74.

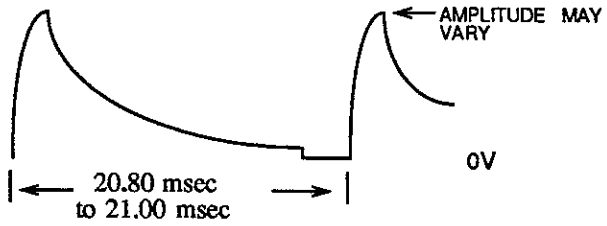


4.3.14 Measure TP3 (A) and TP13 (S/H) with the oscilloscope, verify the following waveforms:



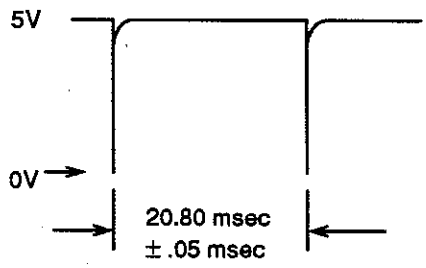
4.3.15 Measure TP8 (VBREF) and TP6 (VBDATA). Verify DC voltages between -20 to -60 VDC.

4.3.16 Monitor TP7 (D CH) and TP9 (R CH), verify the following waveforms:



Check for excessive noise riding on the decay portion of the waveform, this would indicate a problem with the Capnostat™ Sensor or bad connections between the Sensor and the unit.

4.3.17 Scope pin 12 and pin 11 of J3, verify the following waveforms (same for each):



4.3.18 Monitor PIN 9 of J3. Verify a 2 Vp-p digital waveform with no more than 0.5 volt offset from the zero baseline

4.3.19 Remove the sensor from the jack on the front panel, the LED on the 2409 board should flash at half the rate as before (0.5 Hz) and "Sensor Unplugged" should appear in the Capnogram waveform window. Check that the -80 volts TP5 on 2418 (2409) is -12 volts.

4.3.20 Plug the sensor back into the front panel jack, wait for proper temperature to be reached then place the sensor into the ZERO cell (assuming unit is set to calibrate with the Cal Cells). Verify the "Sensor ZERO in Progress" message appears on the screen.

4.3.21 When the ZERO is complete place the sensor into the SPAN cell and wait for the span to complete.
Remove the sensor from the SPAN cell when "Sensor SPAN complete Please remove the sensor from the cell" appears on the screen.
Reinsert the sensor into the SPAN cell when all the messages are cleared from the screen, verify that a steady waveform appears and the "INST CO2" value is equal to that of the SPAN cell reference concentration.

4.3.22 Plug the TB500A sensor simulator into the "SaO2" jack on the front panel, be sure to use the adaptor cable, and set as follows:
SATURATION: **92**

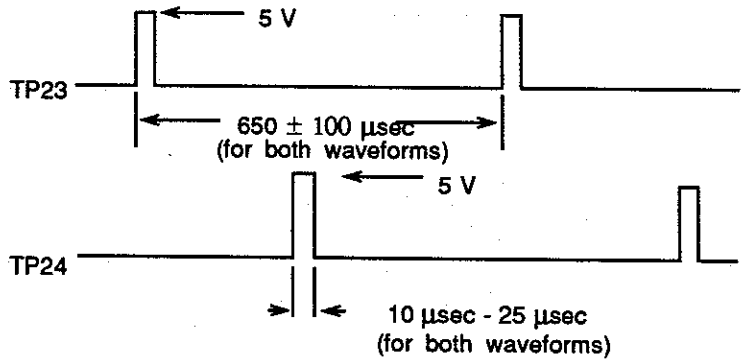
ATTENUATION: 3
POWER: ON

4.3.23 Verify a Plethysmogram waveform appears on the screen with a "Pulse" value of 60 ± 1, and a "SaO2" value of 92 ± 2.

4.3.24 Check the following test points on the 2267 SaO_2 front end board using the D.V.M.
Use the negative lead of C8 on the 2267 board as ground.

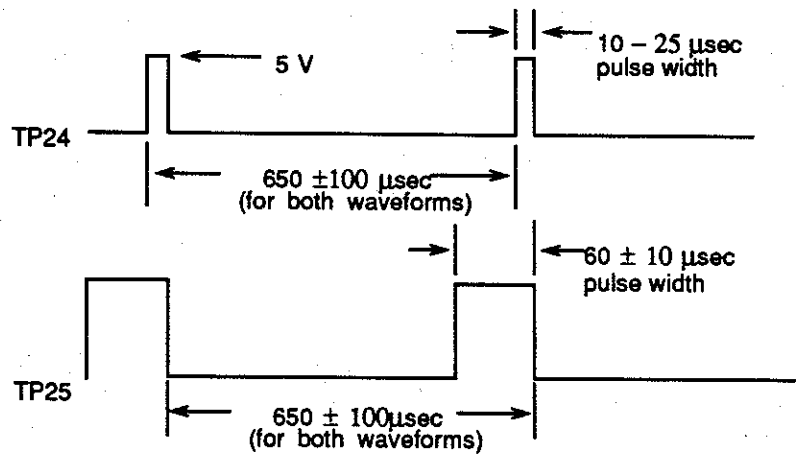
TPA3	+4.9 - +5.2 VDC
TPA5	+4.9 - +5.2 VDC
TPA7	+7.0 - +8.0 VDC
TPA9	-7.0 - -8.0 VDC

4.3.25 Scope pins 23 and 24 on the 2268 board (Referred to as TP23 and TP24) use the negative lead of C8 as ground reference. Verify the following waveforms::



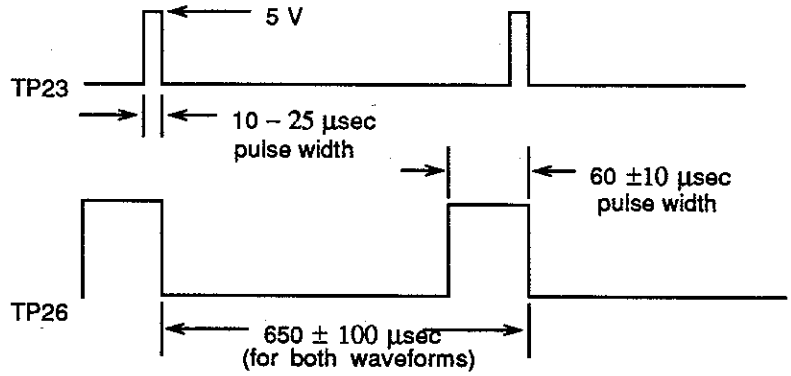
NOTE: Ensure TP24 is out of phase with TP23.

4.3.26 Scope pins 24 and 25.(Referred to as TP24 and TP25). Verify the following waveform parameters:



NOTE: Ensure that the falling edges coincide

4.3.27 Scope pins 23 and 26. (Referred to as TP23 and TP26). Ensure that the falling edge of each waveform coincides. Verify the following waveform parameters.



NOTE: Ensure that the falling edges coincide,

4.3.28 Press and hold the **RED** button on the TB500A, verify "Insufficient Light" and "ALERT" appear on the screen. Release the button.

4.3.29 Press and hold the **INFRARED** button on the TB500A, verify "Probe Error 2" and "ALERT" appears on the screen. Release the button.

4.3.30 Place the SATURATION on the TB500A to **0**, verify "Low Signal Strength" and "ALERT" appears on the screen.
Set the SATURATION back to **92** and check that the waveform reappears, and both "Pulse" and "SaO2" values reappear.

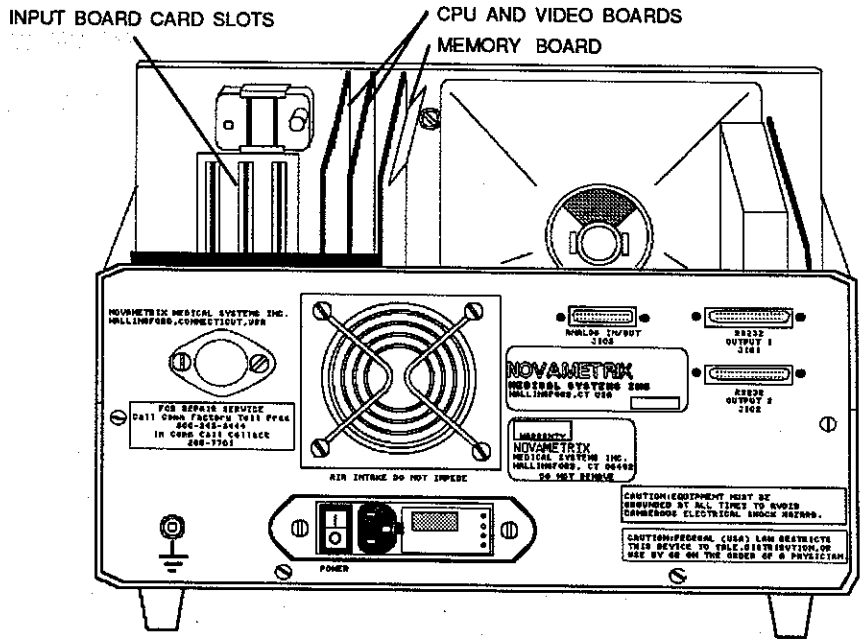
4.3.31 Set the SATURATION control on the TB500A so that it is out of the SaO_2 limits (try both high and low).
Verify that an "ALERT" is shown and that the limit exceeded is flashed on the screen.
Test the alert sound by pressing the **AUDIO** button. Verify a tone is emitted, return the SATURATION to a value within the limits, when the "SaO2" value on the screen is within limits verify the tone stops, then press the **ALERT RESET** button. Both the flashing and "ALERT" should disappear from the screen.

4.3.32 After any repairs or inspections the Safety Checks should be performed when the unit is fully assembled. The Safety Checks are found under Operational Tests.

4.4 Software Updates

There are eight EPROMs associated with the Model 7000 system software. When an update is required either one or all eight EPROMs may have to be changed, this section will describe how to change the software and how to ensure that the each EPROM IC is placed in the proper place. Before removing the top cover ensure that the unit is off and that the line cord is disconnected from the mains supply. The internal electronics of the

monitor and the EPROM ICs are static sensitive devices, follow proper grounding procedures when handling these devices to avoid damage.

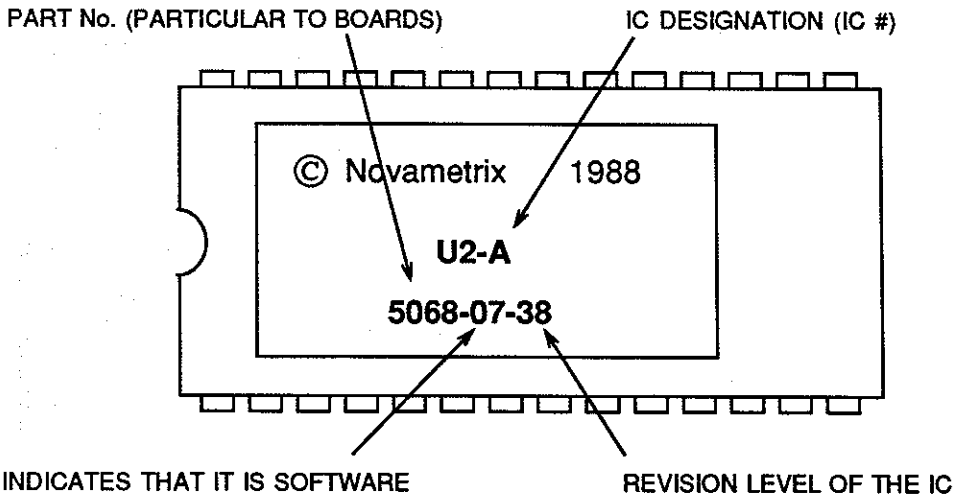


The EPROM ICs have labels which indicate where there are to be placed. It is imperative that they are placed on the proper board, in the proper socket, with proper pin 1 orientation. The following list will describe the part numbering system used, and will show the proper part number to board match.

EPROM Part No.	Circuit Bd.	IC Designation
5012-07-XX	2421 (2407) CO_2 F.E.	U6
5031-07-XX	2404 Video Controller	U22
5031-07-XX	2404 Video Controller	U23
5068-07-XX	2402 CPU Memory Bd	U2-A
5068-07-XX	2402 CPU Memory Bd	U2-B
5068-07-XX	2402 CPU Memory Bd	U3-A
5068-07-XX	2402 CPU Memory Bd	U3-B
5124-07-XX	SaO_2 Front End Bd	U14

NOTE: "XX" DESIGNATES THE REVISION LEVEL OF THE EPROM.

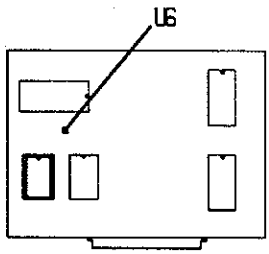
The following is an example of the label that may appear on the EPROM IC. Do not remove this label for any reason for it acts not only as identification of the IC, but also protects the programmed contents from erasure.



Keep in mind that these ICs are static sensitive, do not handle the pins at any time, store them in static protective enclosures only (or conductive foam). Ensure that any personnel handling them is properly grounded, as should be the case whenever any static sensitive devices are handled. This operation should be performed by qualified personnel only, if there are any question contact the Novametrix Service Dept.

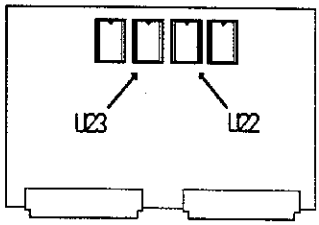
2421 CO_2 Front End Board

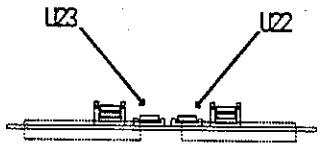
The 2421 Front End board contains one EPROM which is a factory programmed 27C64 device. It is designated as U6 on the board and its part number is 5012-07-XX where "XX" is the program revision level.



2404 Video Controller

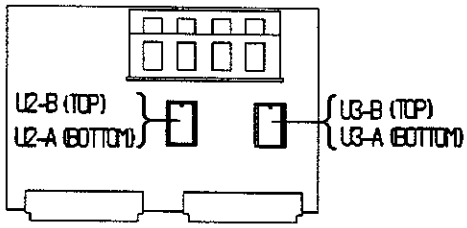
The 2404 Video Controller board contains two EPROM ICs, these are 27C512 devices that are factory programmed. The part numbers are 5031-07-XX where "XX" is the revision level of the ICs. The component designations are U22 and U23.

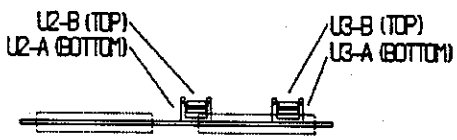




2402 CPU Memory Board

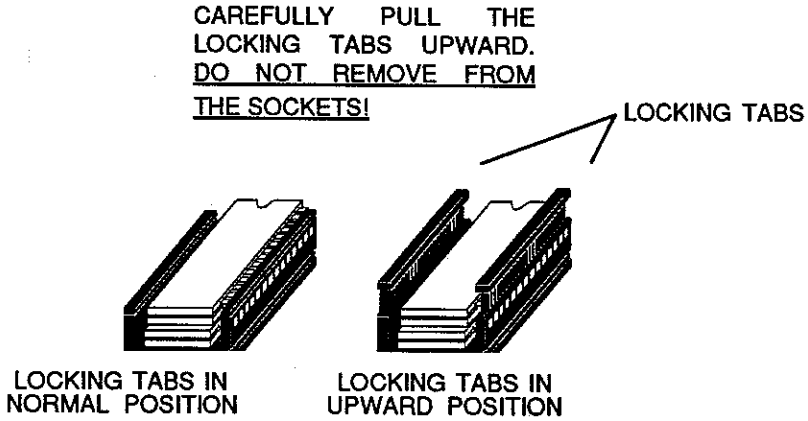
The 2402 CPU Memory board contains the CPU software, this consists of four ICs which are housed in a carrier socket that stacks the two ICs on top of each other in order to consolidate space. When changing these ICs follow the directions carefully to avoid damaging the sockets.



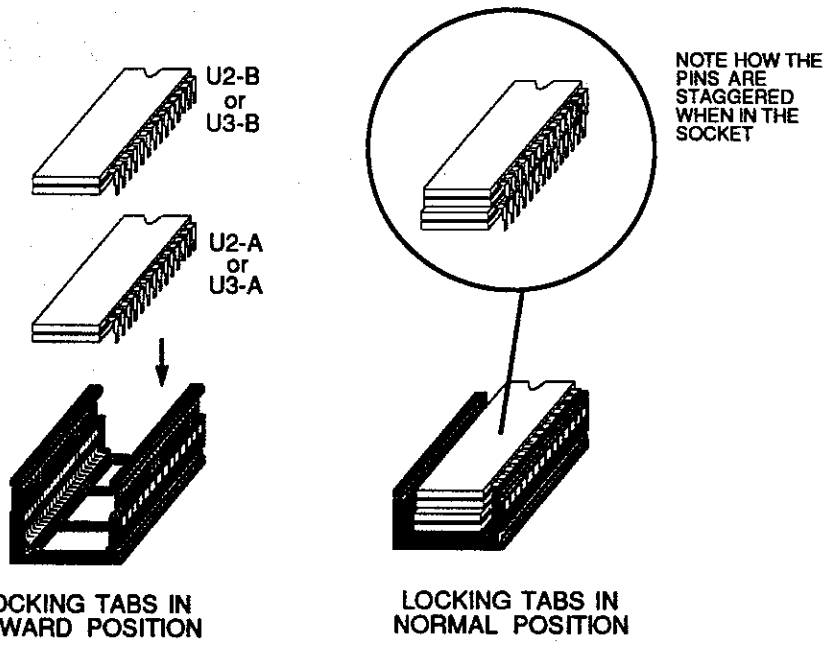


Remove the old ICs in the following manner;

1. Carefully pull the locking tabs upward. *DO NOT REMOVE THE LOCKING TABS FROM THE SOCKETS!* Use an IC Extractor to remove the top IC, pull the IC straight out with even pressure. Repeat for the bottom IC.


CAREFULLY PULL THE LOCKING TABS UPWARD. DO NOT REMOVE FROM THE SOCKETS!
LOCKING TABS
LOCKING TABS IN NORMAL POSITION
LOCKING TABS IN UPWARD POSITION

2. With the Locking Tabs still in the upward position, situate the bottom IC so that the pins align with the socket's bottom contacts. Be sure to observe pin 1's polarity otherwise the IC will fail upon power up. With constant even pressure insert the IC, check that none of the pins are bent, verify that all the pins are properly inserted into the socket's contacts.

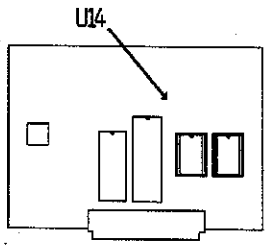

U2-B or U3-B
U2-A or U3-A
NOTE HOW THE PINS ARE STAGGERED WHEN IN THE SOCKET
LOCKING TABS IN UPWARD POSITION
LOCKING TABS IN NORMAL POSITION

3. Place the top IC so as to align the pins with the top IC contacts. With steady, even pressure insert the IC, be sure to observe proper pin 1 orientation. When both ICs are in place and all the pins are

properly seated in the socket, slowly press the locking tabs back into their normal positions.

SaO2 Front End Board

The SaO2 Front End Board contains one factory programmed EPROM, it is a 27C64 device designated as U14 on the 2267 board. The part number is 5124-07-XX where "XX" is the revision level of the EPROMs program.

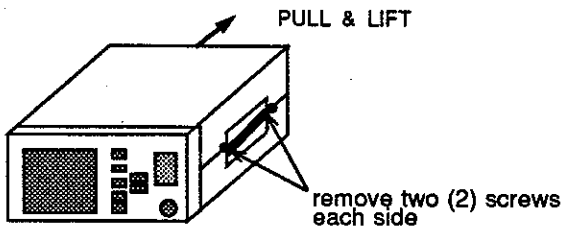


4.0 Assembly and Disassembly Instructions

4.1 Disassembly

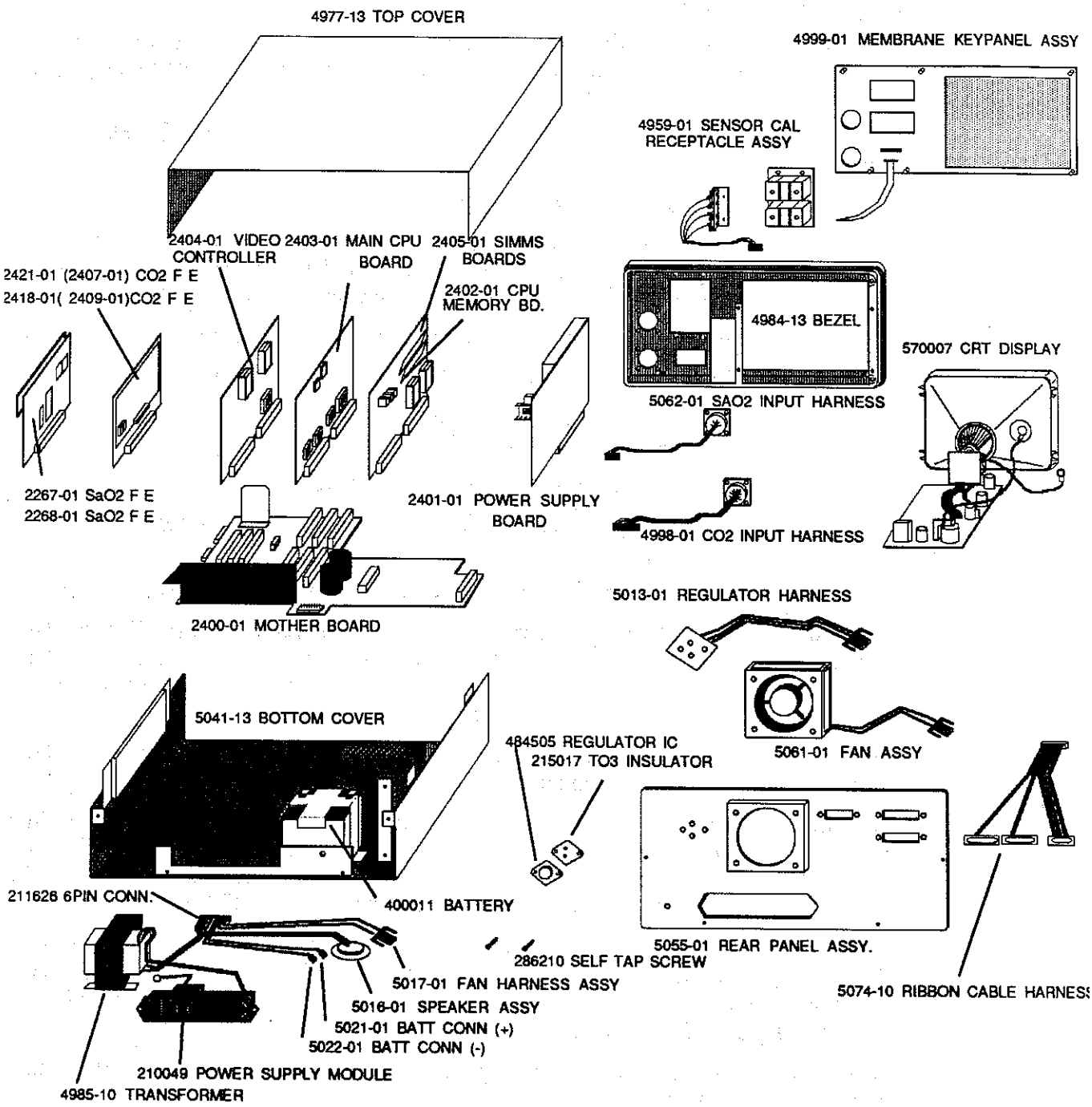
Before attempting to disassemble the Model 7000 disconnect the power cord from the mains supply to avoid possible electrical shock. Ensure that all external equipment and sensors are unplugged from the unit. Follow proper grounding procedures when handling electronic components and circuit boards to avoid damage to static sensitive devices.

The top cover is removed by loosening two screws on either side of the monitor, then sliding the cover off from the rear of the unit. The inside of the unit is arranged as follows:



- The three digital boards (Main CPU, Memory, and Video Controller) are housed in the three 8 1/4" card slots located to the right of the CRT (looking from the front of the unit). These boards are removed by carefully pulling the boards directly out of the card slots.
- The two Front End Boards are located in the 7" card slots, these are removed in the same manner, simply pull the boards directly out of the card guides. Both the CO_2 and the Saturation Front End Boards are dual board assemblies (they both contain piggyback boards).
- The Power Supply board is contained in its own card guide located to the left of the unit (looking from the front). To remove this board unplug the connector which runs from this board to the CO_2 Front End Board, then simply slide the board out from the card guides.
- The CRT is easily removed simply unscrew the front panel by loosening the five screws (three on the bottom panel, one on either side) which hold the Front Panel to the chassis. Once the Front Panel is loose the CRT/Front Panel assembly can be pulled forward to enable easy removal of the four screws (two located on either side) holding the CRT. The CRT circuit board is removed from the Motherboard assembly by removing the four screws which hold it in place, then slide it off the edge connector J213.
- The battery is held in place by a black anodized bracket. This bracket is removed by loosening the four nuts and sliding it off the battery.
- The Motherboard is held in place by eight (8) screws. Once these are removed the board is easily lifted from the chassis after the removal of six (6) connectors (J211, J212, J217, J214, J215, J216).
- There are four screws which hold the rear panel to the chassis. The fan, regulator, J101, J102, J103, and a ground lug are also attached to the rear panel (all are easily disconnected through connectors in the system).

Assembly Diagram



4.2 Assembly

The assembly of the Model 7000 is simply the disassembly in reverse. Ensure that all power is removed from the unit before attempting to assemble it.

- Before reinstalling the Motherboard check that the two grounds (one from the rear panel, one from the power entry module) are securely screwed in place. Ensure the Motherboard is securely set in place by eight (8) screws.
- The battery can be replaced by simply replacing the bracket which holds it in place.
- The following connections are to be plugged into the Motherboard:
  - Six (6) pin connector from the transformer/battery/fan into the six (6) pin receptacle marked J212, and the two pin connector from the speaker plugs into the two pin housing marked as J212.
  - The connector from the rear panel mounted regulator into J217.
  - The connector from J102-103 on the rear panel into J211.
  - Aluminum ribbon strap from the front panel assembly should be tied to one of the screws which hold the Motherboard down.
  - The connector from the Cal Cell into J215.
  - The connector from the CO_2 (black) receptacle on the front panel into J216.
  - The ribbon cable from the front panel assembly into J214.
- Re-install the CRT board and screw in place. Then re-attach the CRT to the front panel assembly, be sure to attach the black ground wire to one of the screws that hold the CRT in place. The Front Panel assembly may be screwed back in place at this time.
- Slide the Power Supply Board in place, the 64 pin connector is polarized so the components on the board face the inside of the unit.
- The digital boards can be installed at this point. The boards can be plugged in only one way into each of the connectors, however the order is irrelevant. It is required that the Memory board be placed in the leftmost slot (from the front of the unit) because of the clearance necessary for the two SIMMS boards.
- The CO_2 Front End Board should go into the leftmost 7" card slot, this will allow enough clearance for the Saturation Front End Board to be placed in the rightmost slot. Verify that the connector from the green SaO_2 front panel receptacle is plugged into the SaO_2 Front End Board.
- The cover simply slides on from the rear of the unit and is secured via the four screws on either side.

Whenever the monitor is disassembled all safety checks should be performed by qualified personnel to ensure the integrity of the unit. Refer to the Operational Tests section for Safety Checks instructions.

5.0 Specifications

5.1 General

Below are the specifications for the Novametrix SaO2/ETCO2 Monitor Model 7000. These specifications are listed for informational purposes only. The specifications are subject to change without notice.

5.2 The Capnostat™ Sensor

- Sensor Type
  "On-airway" (mainstream) system
- Principle of Operation
  NDIR, dual wavelength ratioing, no moving parts
- Measurement Range
  0-99 mmHg CO_2
- Accuracy
  0-40 mmHg, ±2 mmHg
  40-100 mmHg, ±5% of reading
- Stability
  ±2 mmHg (at zero, 8 hour period)
- Sensor and Adapter Construction
  durable, glass filled ABS, ultra-flexible cable
- Weight of Sensor and Adapter
  less than 1 oz. without cable
  less than 6 oz. with cable and connector
- Airway Adapter
  Disposable or reusable, less than 5cc dead space, meets ANSI Z-79
- Sensor Size
  1 3/4" x 1 1/2" x 3/4"; 12 foot cable
- Moisture Resistant
  Sensor sealed against moisture
- Shock Resistant
  Sensor will withstand 6-ft. drop to tile floor
- Step Response Time
  less than 100 milli-seconds
- Warm Up Time
  less than five (5) minutes

5.3 Oxygen Saturation SaO2 Sensor

- Range
  0-100%
- Accuracy
  100-80% ±2% of reading
  85-50% ±3% of reading
  50-0%, unspecified
- Resolution
  1%
- Display Averaging Time
  Menu selectable, 2, 4, 8, 16 seconds
- Audible Trend Feature
  Tone of audible pulse varies with displayed SaO2 value.
- Alert Limits
  High limit; 5-100%
  Low limit; 0-95%
- Pulse Rate Range
  30-250 beats per minute
- Pulse Rate Accuracy
  ± 1% of full scale
- Pulse Rate Resolution
  1 beat per minute
- Pulse Rate Display Averaging Time
  Menu selectable, 2, 4, 8, 16 seconds
- Pulse Rate Audible Trend Feature
  Tone of audible pulse varies with displayed SaO2 value.
- Pulse Rate Alert Limits
  High limit, 35-250 beats per minute
  Low limit, 30-245 beats per minute

5.4 The Monitor

- Display
  7-inch diag. CRT
  0-100, 0-50 menu selectable scale
- CO_2 Display Resolution
  0-50 scale, 0.25 mmHg
  0-100 scale, 0.50 mmHg
- Respiratory Rate Resolution
  ±1 breath per minute
  0-150 respiration/minute
- Respiratory Interval Detection Period
  fixed at 30 seconds
- Calibration
  Zero and Span calibration with external sealed gas cells or user selectable CO_2 flowing gas at 5% or 10%
- N_2O/O_2 Compensation
  No more than 2 mmHg error, operator selectable
- Barometric Pressure Compensation
  No more than 2 mmHg error, operator selectable
- Alert Limits
  Operator selectable (Automatic or menu selectable)
  End Tidal CO_2: low and high
  Respiratory Rate: low and high
  Respiratory Interval Delay: 30 seconds
  Visible alert is immediate
  Audible alarm occurs 10 sec. after violation of set limit.
- 2 Minute Silence
  When AUDIO key is pressed, deactivates audible alerts for two minutes. Indicated by illuminated 2 MIN LED.
- Audio Off
  Press and hold AUDIO key for 3 seconds, will deactivate audible alerts. Indicated by illuminated OFF LED.
- Digital Data Output
  Provides RS232 data output compatible with;
  RS232C computer interface
- Analog (Recorder) Data Output
  Provides analog output for external strip chart applications
  Respiratory Rate Value,
  CO_2 Value,
  CO_2 Waveform,
  Pulse value,
  SaO_2 value*
  Plethysmogram waveform
- Trend Memory
  Menu selectable trending memory times of;
  20 minutes, 1 hour, 4 hours, 8 hours.
- Operating Environment
  10-40° C (50-104° F)
  0-90% relative humidity (non-condensing)
- Monitor Size
  Height: 5.5 in.(13.97 cm)
  Width: 13.9 in.(35.24 cm)
  Depth: 13.4 in.(33.97 cm)
- Monitor Weight
  21 pounds (9.53 kg)
- Power
  100/120/220/240 vac ±10%, 50/60 Hz
  (must be specified at time of order)
- Fuse Rating
  U.S. Specification, 2 ampere slow-blow
  European Specification, 1 ampere 250V (x2)
- Battery
  Type, lead-acid gel-cell
  Battery Life, 1 hour
  Recharge time, battery fully recharged in 8 hours max.

5.5 Options*

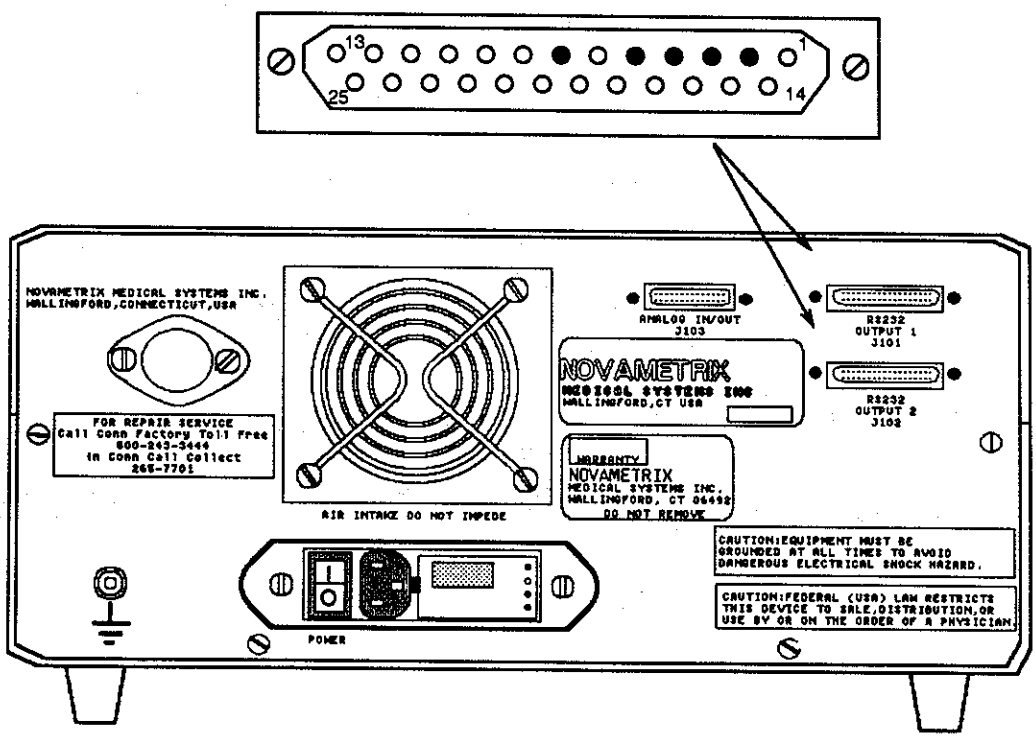
- Sampling Attachment
  Allows gas sampling for non-intu bated patient applications
- Neonatal Adapter
  less than 1 cc dead space
- * - scheduled for release in the summer of 1988

6.0 Connecting External Equipment

6.1 RS-232 outputs

The Model 7000 has two jacks (J101, J102) on the rear panel for RS-232 communication between itself and an external device. These are connected to IC18 and IC19 on the Main CPU Board and transmit serial communication from the external device to the MC68000 microprocessor. The pinout is as follows:

JACK-PIN	FUNCTION
J101-2	DATA IN 3
J101-3	XMITT 3
J101-4	RTS 3
J101-5	CTS 3
J101-7	GND
J101-24	+5 VOLTS
J102-2	DATA IN 4
J102-3	XMITT 4
J102-4	RTS 4
J102-5	CTS 4
J102-7	GND



6.2 Analog In / Out

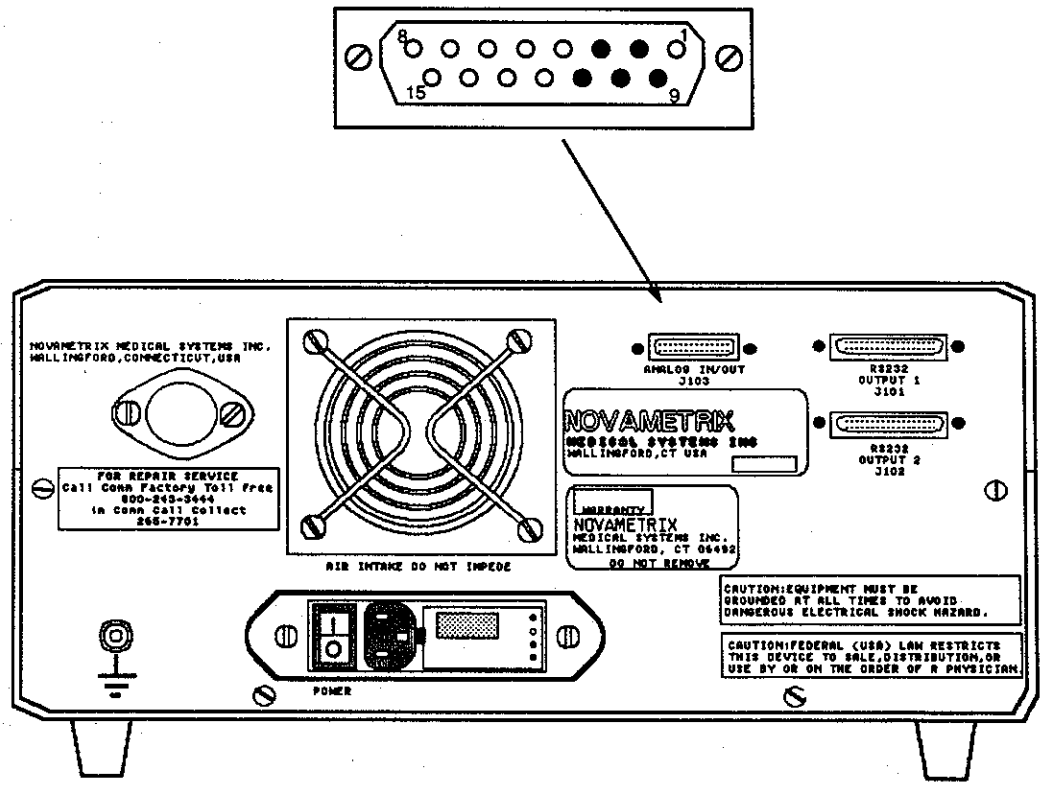
6.2.1 Analog In

The Analog Input on the Model 7000 is not enabled through the current software. In a future software release the inputs will be enabled and utilized through J103 on the rear panel of the monitor. It will consist of three channels that can take an analog voltage of ±10 volts then digitize them to be processed by the MC68000 microprocessor.

6.2.2 Analog Output

The Analog Output of the Model 7000 consists of three output channels which the user can assign to one of six parameters through the front panel softkeys. The outputs are located on J103 on the rear panel and is labeled "ANALOG IN/OUT". The pinout is as follows:

CHANNEL	J103 PIN #
CH1	2
CH2	10
CH3	9
GROUND	3 &11



These channels can be assigned to any one of six parameters in the Model 7000. The type of output will depend on the specific assignment of the channel, the 8-bit Digital to Analog Converter (DAC) used for these outputs can produce an analog voltage from 0 to 5 volts. The scale for each of the parameters is broken down as follows:

PARAMETER	RANGE	OUTPUT SCALE
Capnogram	0-100 mmHg	0-3.92 volts (19.6 mv/0.5 mmHg)
End Tidal	0-100 mmHg	0-1.96 volts (19.6 mv/mmHg)
Resp. Rate	0-200 br/min	0-3.92 volts (19.6 mv/br/min)
Plethysmogram	0-100	0-2.49 volts maximum output
Saturation	0-100	0-1.96 volts (19.6 mv/%)
Pulse Rate	0-250	0-4.96 volts (19.6 mv/bts/min)

The voltages at these outputs can be measured at ZERO, HALF, and FULL scale when in the "ANALOG CALIBRATION MENU" by simply pressing the **Toggle Scale** softkey until the desired scale is reached. To get to the "ANALOG CALIBRATION MENU"

- Press **System Control** from the real-time display (waveform or digital).
- Select **Setup** from the "CONTROL MENU".
- Press **Interfaces**, then **Analog Output** softkeys. When the "ANALOG OUTPUT" window appears press **Calibrate Channels** (this assumes that the channels have already been assigned, if not then press **Select Channels** to assign parameters to the different channels).

A more in depth discussion on setting the channels up for the different parameters is explained in the Operators Manual. The unit will select the default assignments should the backed up memory lose power or be replaced, the same will occur if the unit is powered up in the default mode.

7.0 Troubleshooting Guide

7.1 Error Messages

If a sensor related error condition is detected, the Model 7000 will display an error message on the display screen. The error messages are listed below.

Sensor Not Calibrated ..... Sensor has not been calibrated—calibrate
Sensor has been disconnected then reconnected—recalibrate

Sensor Unplugged ..... Sensor not connected to monitor—connect sensor
Sensor or sensor cable faulty—replace sensor

Sensor Over-Temp ..... Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel

Probe Faulty ..... Note: This message may be displayed at power-up (with sensor connected). The message should disappear as the monitor and sensor warm up (approximately 30 seconds).
Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel

Check Airway ..... Sensor not up to temperature—wait until sensor warms up
Sensor not connected to airway adapter or cal cells
Optical path blockage—check that airway adapter windows are not contaminated, check sensor is properly seated on the airway adapter
Calibration error—retry calibration
Calibration cell error—try gas calibration
If doing gas calibration—CO_2 concentration too high
Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel

Reference Error ..... Sensor not up to temperature—wait until sensor warms up
Optical path blockage—check that airway adapter windows are not contaminated, check sensor is properly seated on the airway adapter
Calibration error—retry calibration
Calibration cell error—try gas calibration
If doing gas calibration—CO_2 concentration too high
Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel
Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel

Not up to Temp ..... Sensor not up to temperature—wait until sensor warms up
Sensor faulty—do not use, replace sensor
Monitor faulty—do not use, contact qualified personnel

Zero Cal Error ..... Calibration error—retry calibration
Optical contamination—clean Zero Cell and sensor windows

Zero Cell failure—contact qualified personnel (use gas cal)
If gas cal, Zero Cal attempted while CO_2 is present or optical contamination—clean airway adapter and sensor windows
Sensor faulty—replace sensor

Span Cal Error ..... Calibration error—retry calibration
Optical contamination—clean Span Cell and sensor windows
Span cell value on cell matches value set in software?
Span Cell failure—contact qualified personnel (use gas cal)
If gas cal, Zero Cal attempted while CO_2 is present or optical contamination—clean airway adapter and sensor windows
Sensor faulty—replace sensor

Data Transfer Error ..... Monitor faulty—do not use, contact qualified personnel

Sync Error ..... Monitor faulty—do not use, contact qualified personnel

Probe Error 2 ..... Red LED on SaO2 sensor nonfunctional—check for object obstructing light path.
Sensor faulty—replace sensor.

Probe Error 4 ..... Infra-red LED on SaO2 sensor nonfunctional—check for light obstruction.
Sensor faulty—replace sensor.

The following section is intended to help determine the possible cause of problems one might encounter when operating the Model 7000. It is by no means a complete problem diagnostic listing but will help in determining whether the problem is:

- Minor component failure, i.e. battery, fuse.
- Major component failure, i.e. internal electronics.
- Incorrect setup, i.e. wrong mains fuse setting.
- Bad environment, i.e. electrical interference, poor powerlines.

-The unit will not turn on,

- verify the line cord is attached and undamaged, mains power switch on the rear panel is in the | position and the green "AC" LED on the front panel is illuminated (assuming no battery backup).
- check the fuse inside the power entry block where the line cord is attached.
- check battery voltage,
- power supply board (or other board) jarred loose from its card holder (possible shipping damage).
- wrong mains voltage setting, check power entry module.
- Sensor loading down the power supply, try powering up with the sensors disconnected.

NOTE: If the unit continually blows fuses when powered on or when on for a period of time contact Novametrix Service Dept. for assistance.

-Unit intermittently turns off by itself,

- unit is running on battery power (or AC power was interrupted), and the battery voltage is dropping below its threshold level,

-CRT jitter, unsteadiness,

- battery voltage low or battery is disconnected (or dead).
- CRT requires alignment.
- external electromagnetic interference.

-Monitor will not respond to button or softkey commands,

- CPU lockup, try powering down then powering up again.

-Unit will not calibrate when sensor is placed into ZERO cell,

- unit is programmed to calibrate with gas.
- Zero cell switch is defective,
- Capnostat™ CO_2 sensor not properly fitted into ZERO cell slot.